

# PCB STACK UP

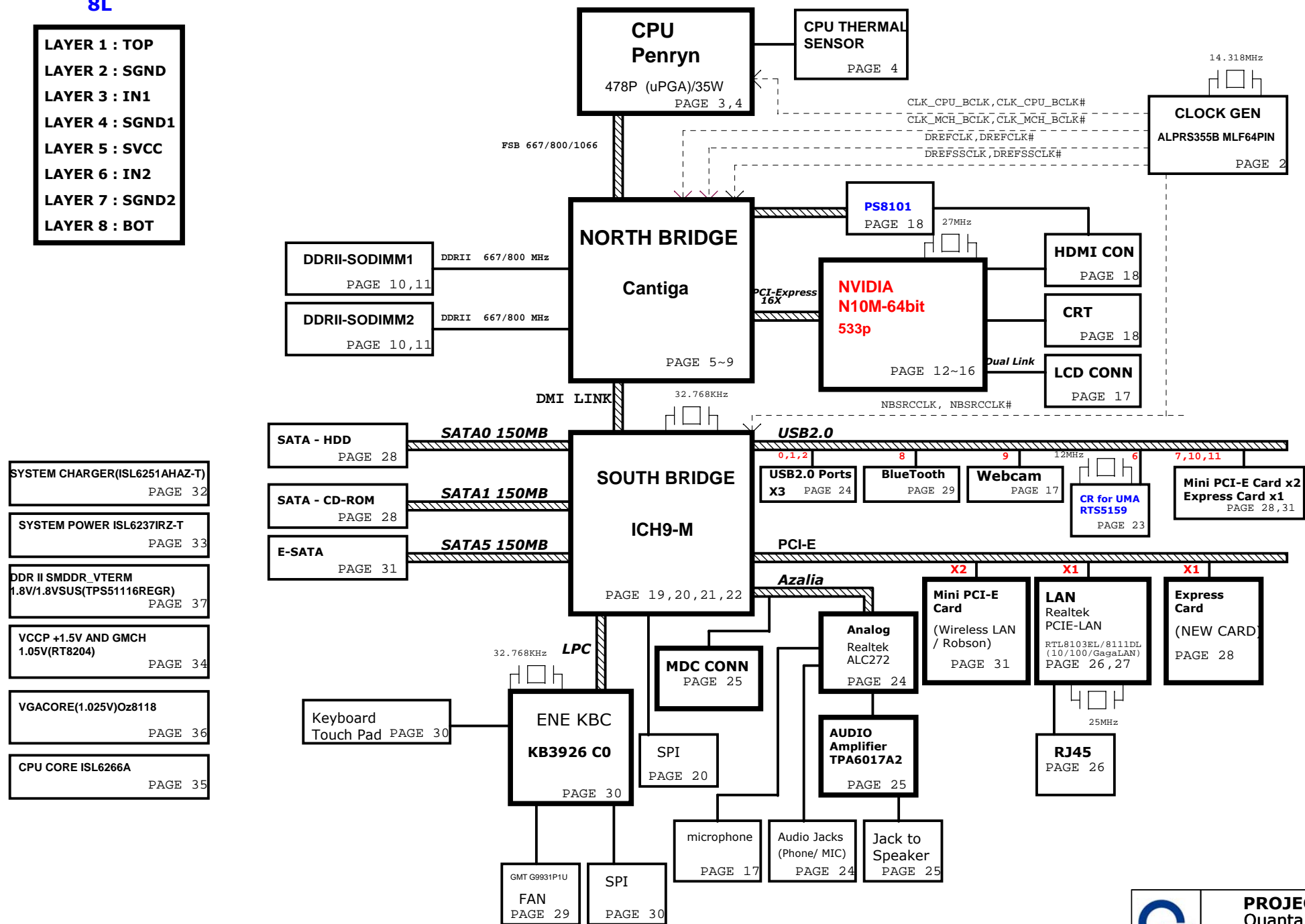
8L

LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1  
LAYER 4 : SGND1  
LAYER 5 : SVCC  
LAYER 6 : IN2  
LAYER 7 : SGND2  
LAYER 8 : BOT

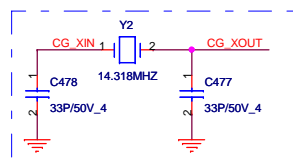
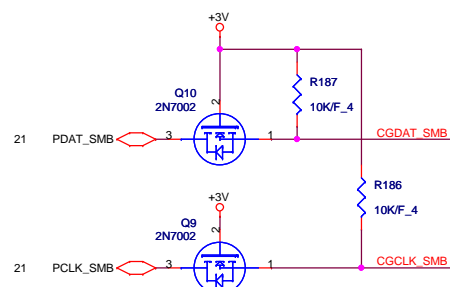
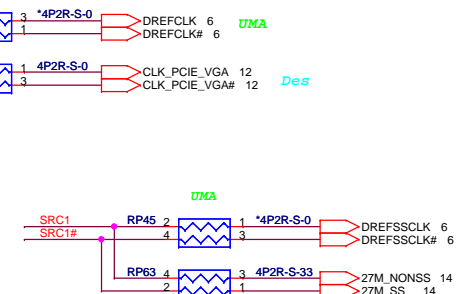
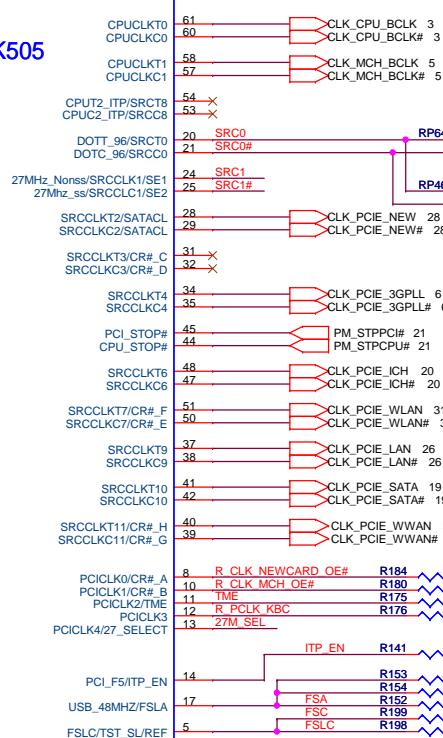
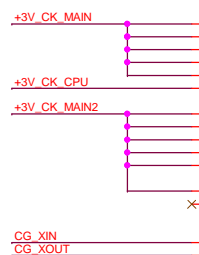
## Preso-II

## BLOCK DIAGRAM

01

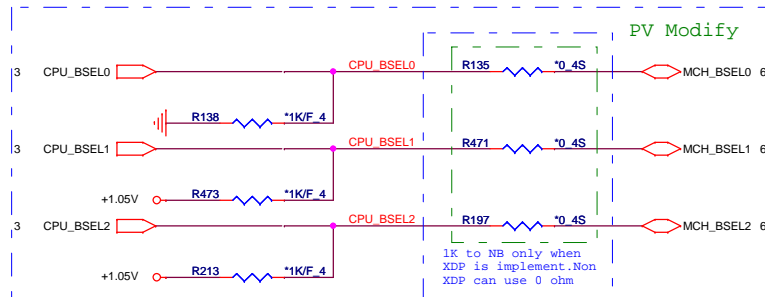
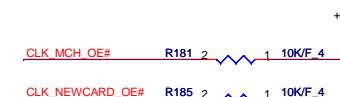




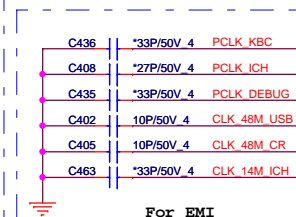


27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

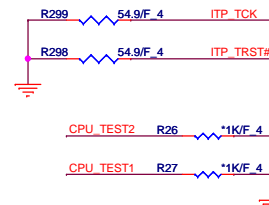
ICS	ICS9LPRS355BKLF	ALPRS355000
Silego	SLG8SP513VTR	AL8SP513000
Realtek	RTM875N-606-VD-GR	AL000875000



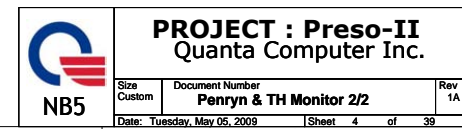
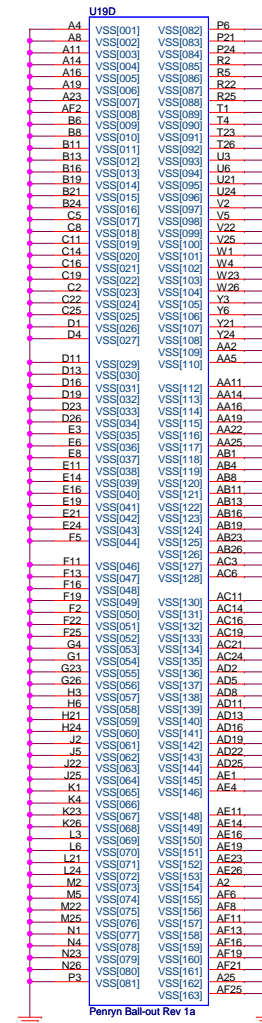
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33



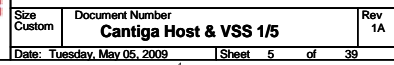








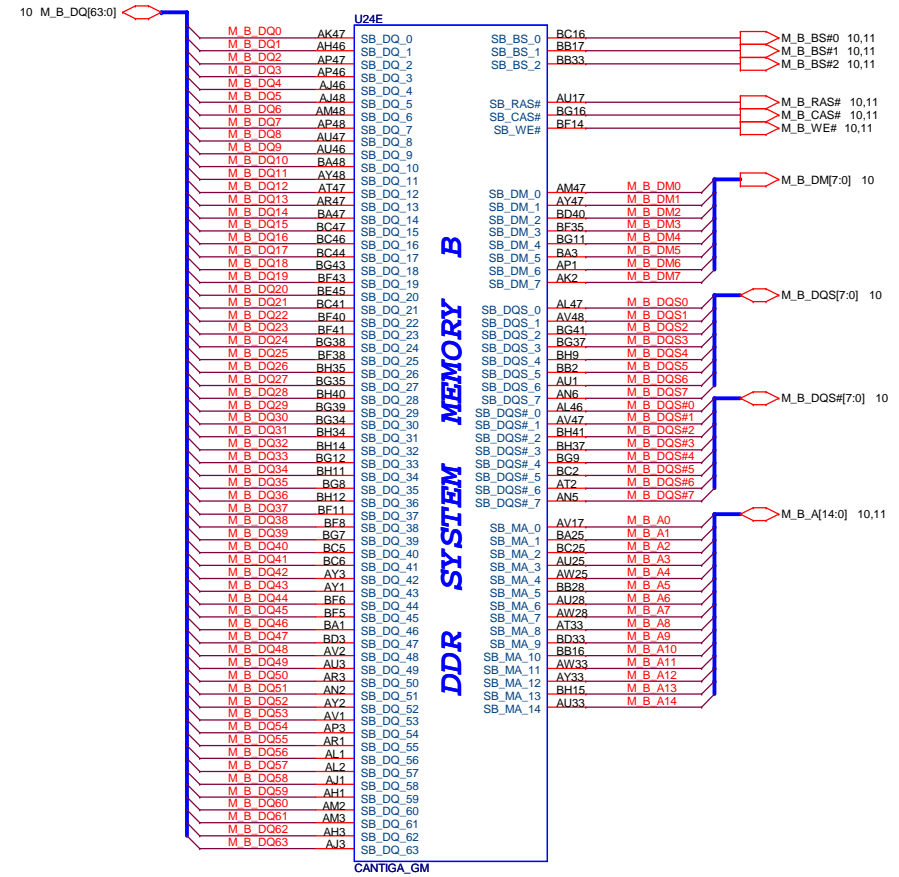
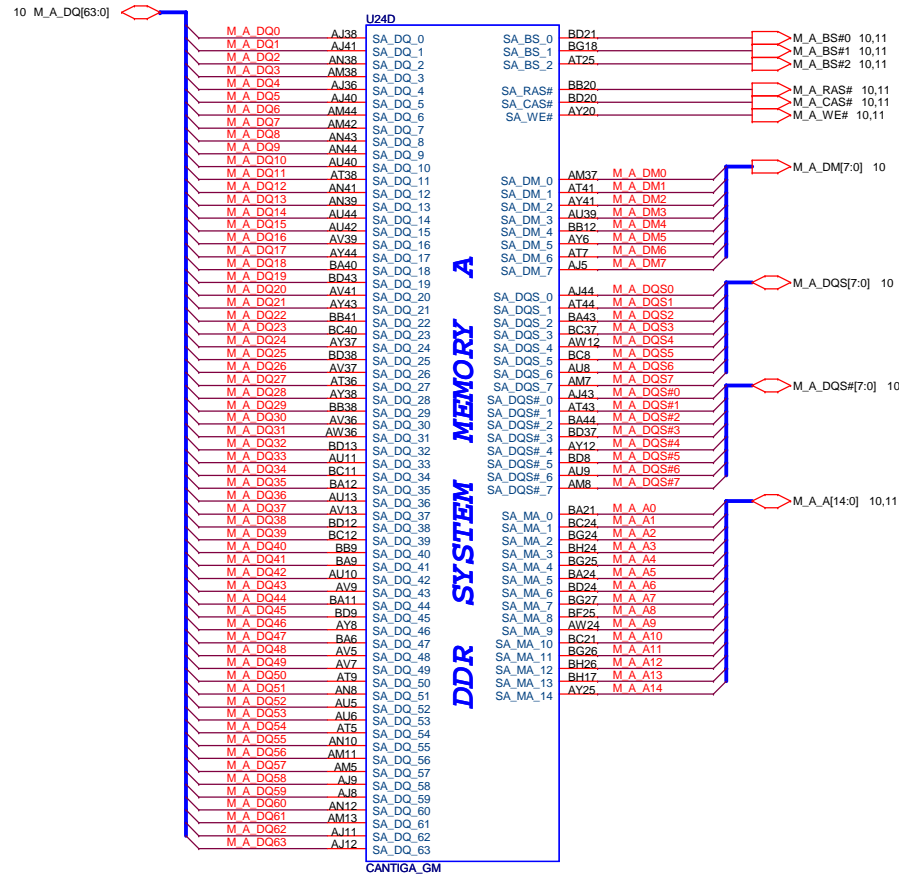












**PROJECT : Preso-II**  
**Quanta Computer Inc.**

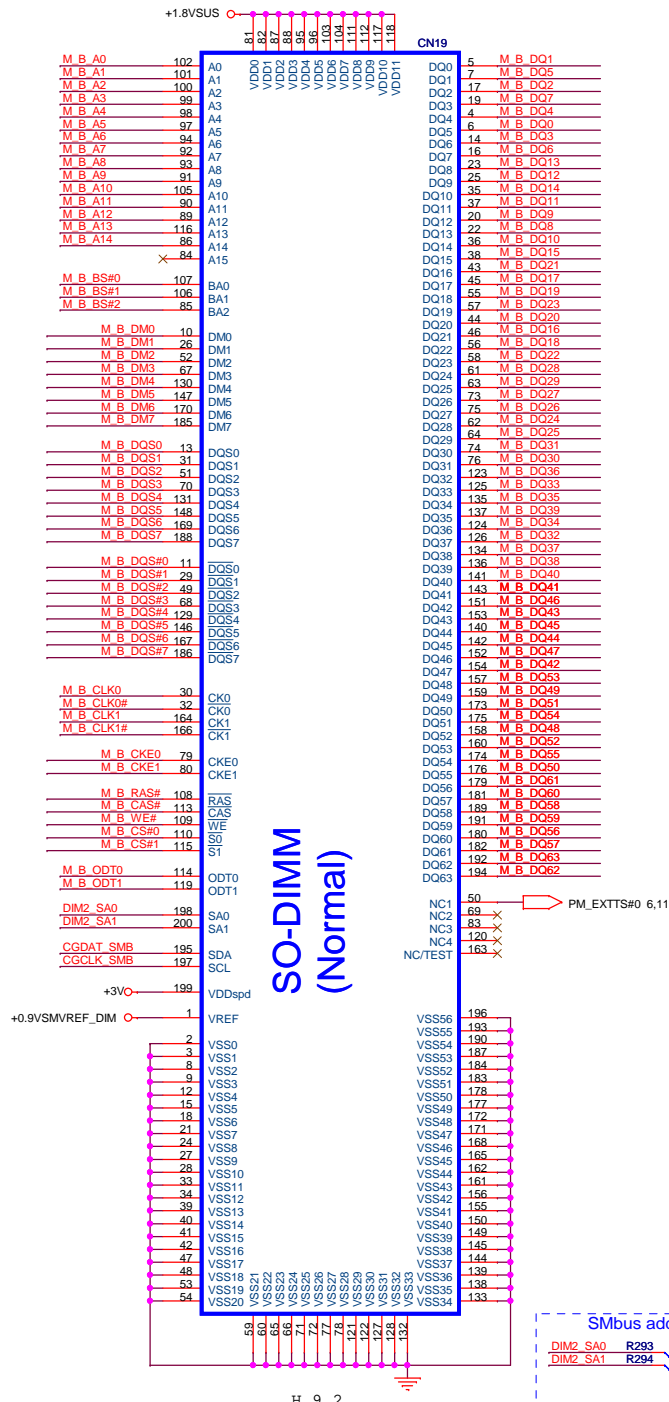




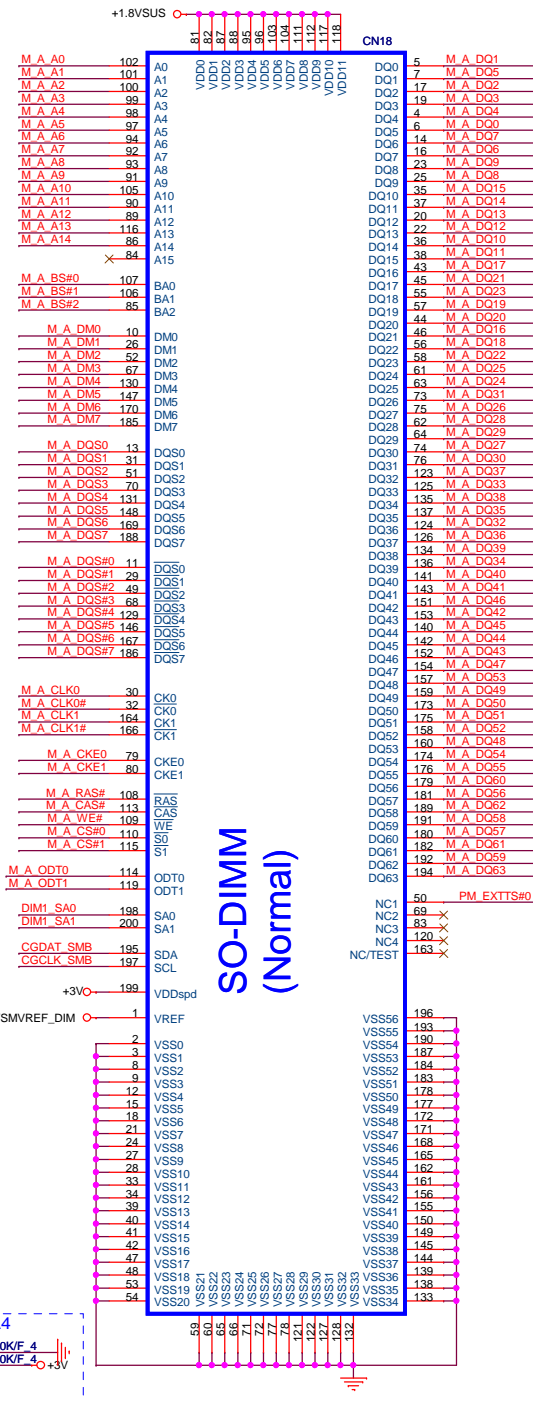




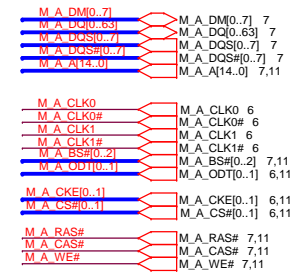
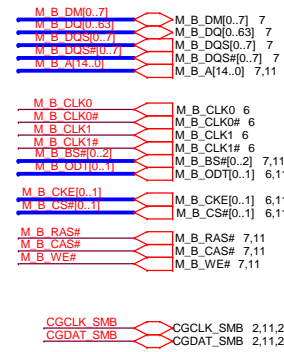




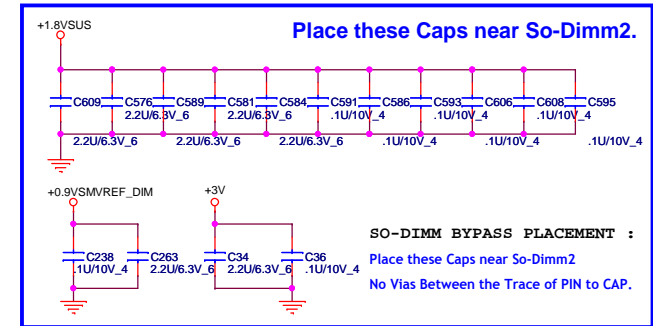
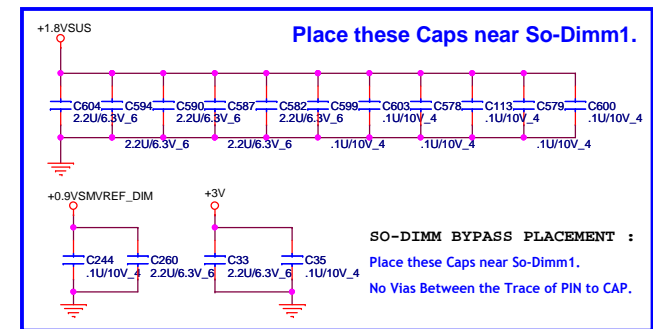
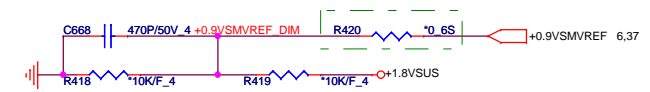
H 9.2



H 5.2



PV Modify

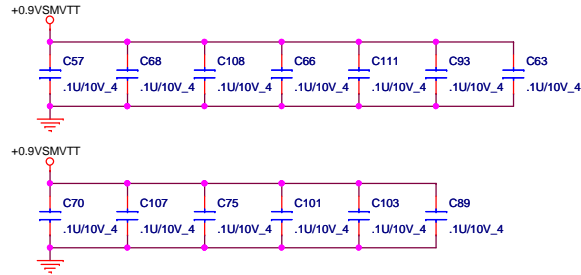


**PROJECT : Preso-II**  
Quanta Computer Inc.

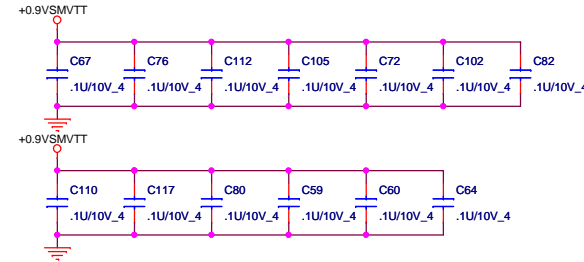


# DDRII DUAL CHANNEL A,B.

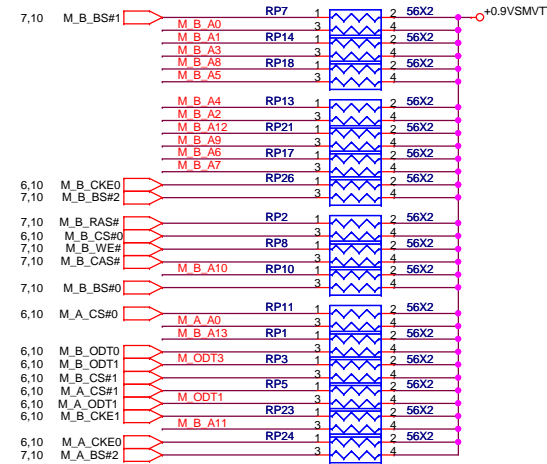
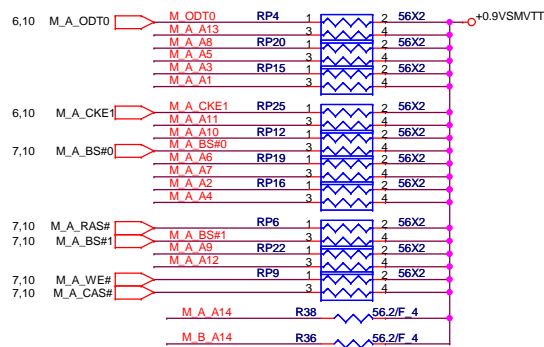
## DDRII A CHANNEL



## DDRII B CHANNEL

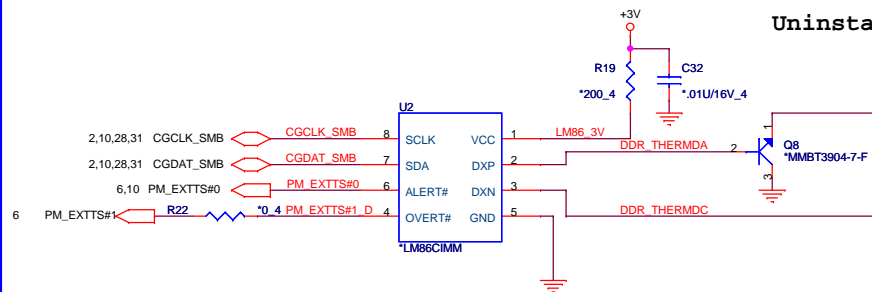


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR\_VTERM



M\_B\_A[14..0] M\_B\_A[14..0] 7,10  
M\_A\_A[14..0] M\_A\_A[14..0] 7,10

Uninstall



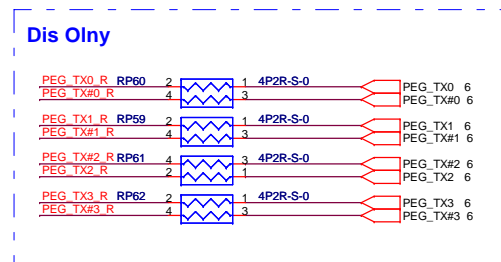
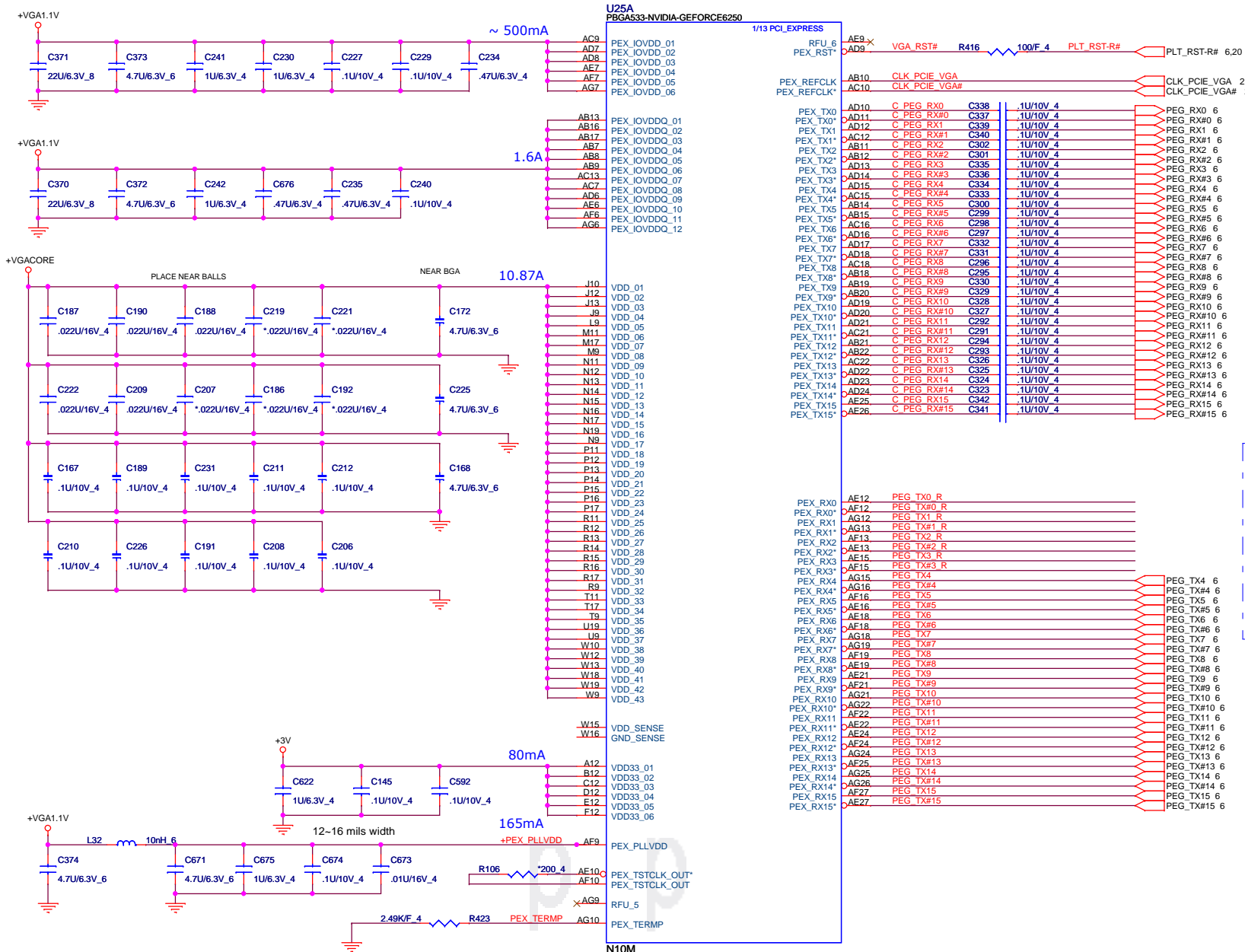
+0.9VSMVTT 37  
+3V 2,4,6,9,10,12,14,15,17,18,19,20,21,22,24,25,26,28,29,30,31,35,36,38



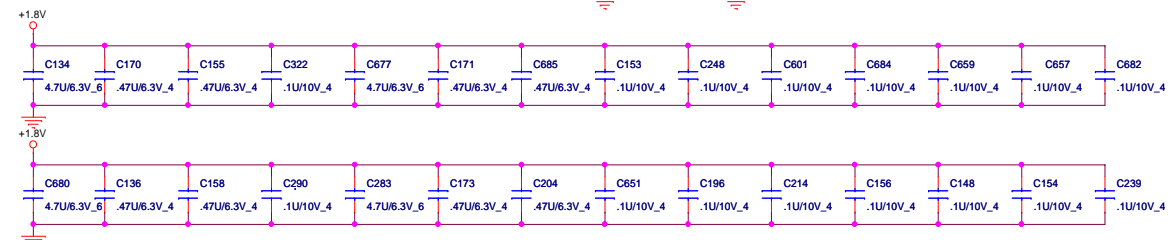
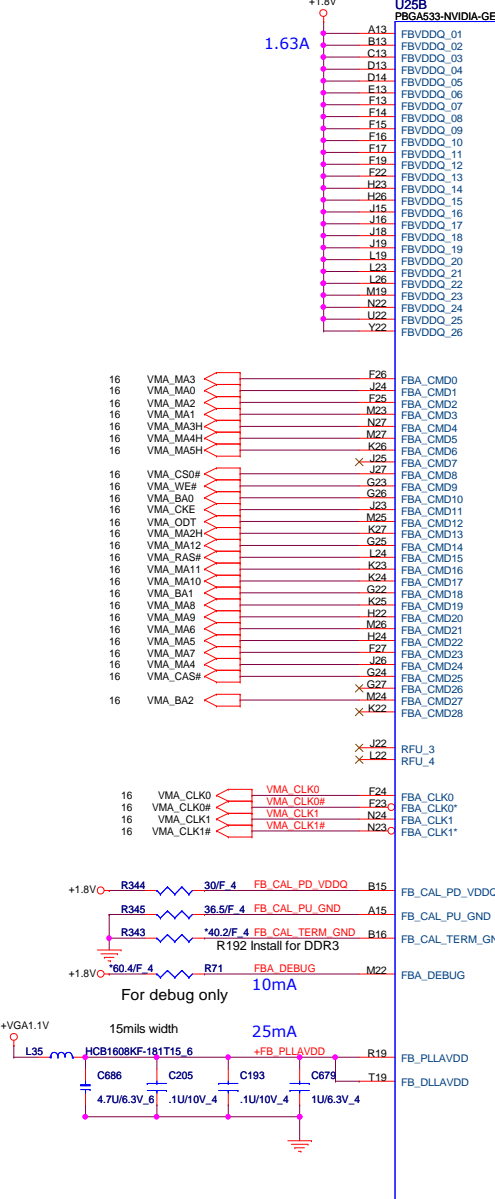
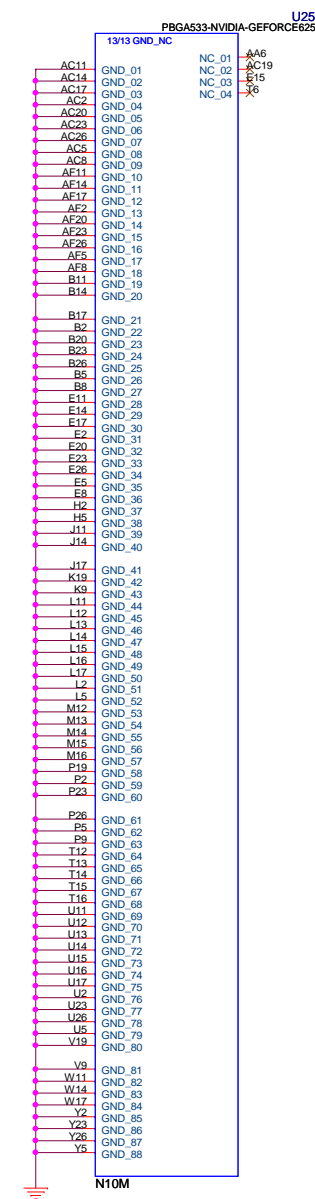
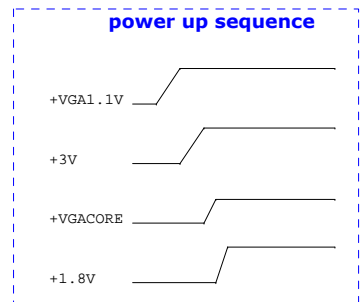
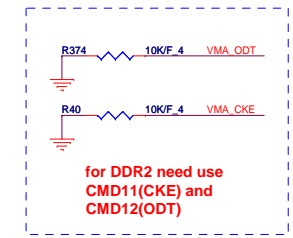
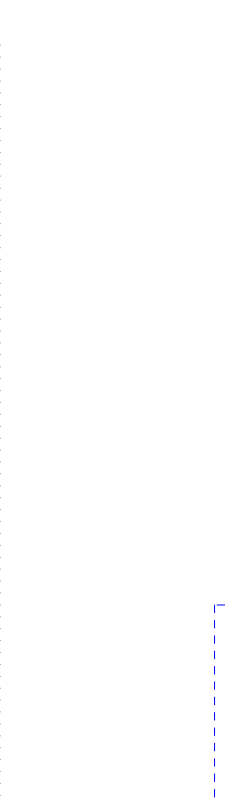
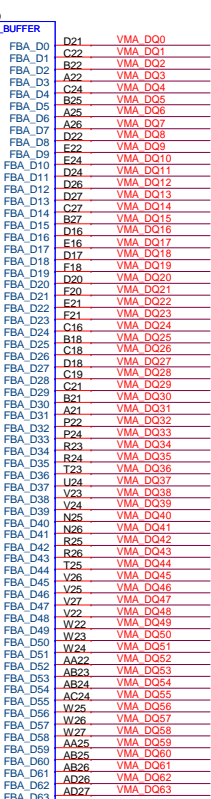
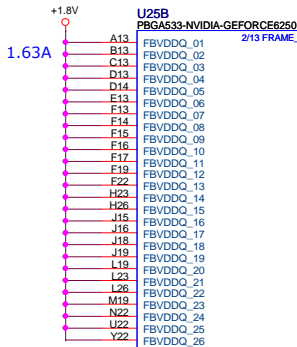
**PROJECT : Preso-II**  
Quanta Computer Inc.

Size Custom	Document Number DDR2 termination	Rev 1A
Date: Tuesday, May 05, 2009	Sheet 11 of 39	

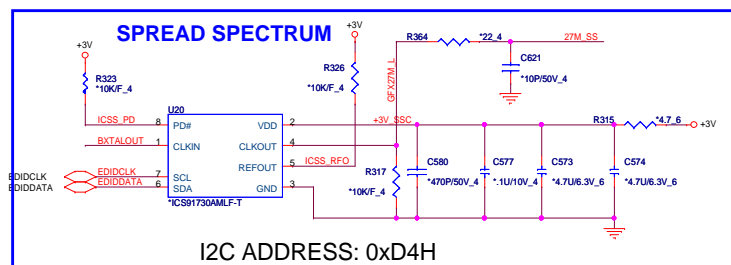
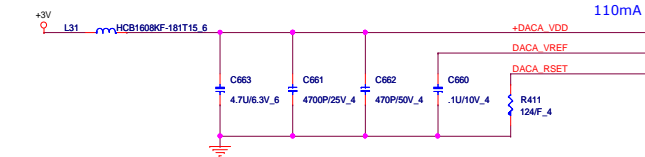
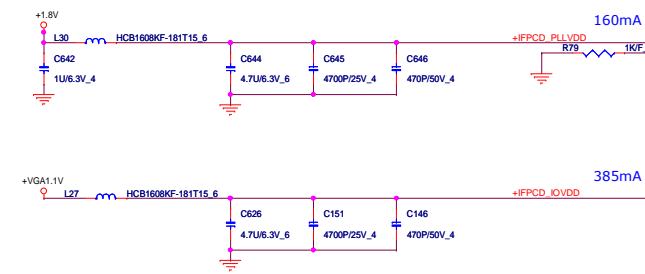
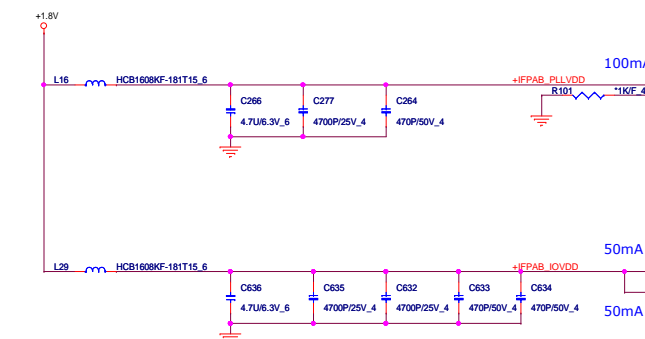
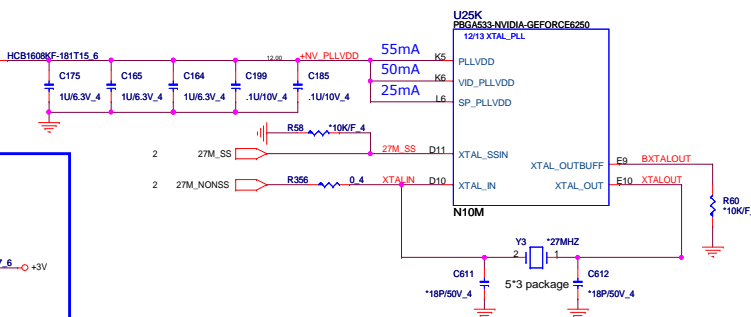
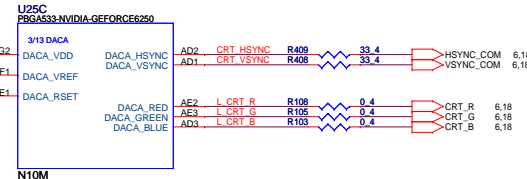
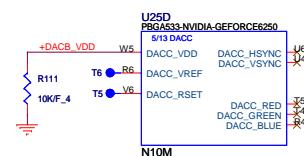
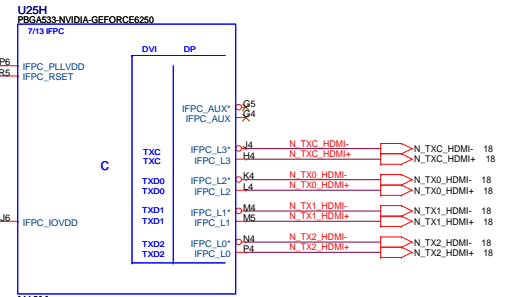
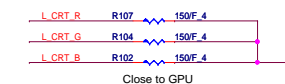
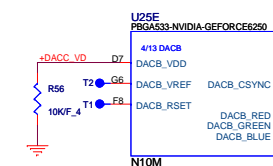
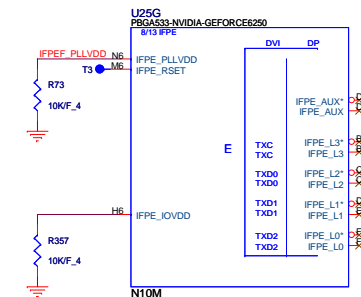
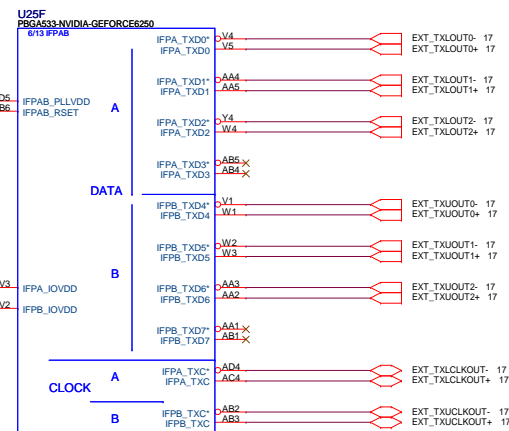








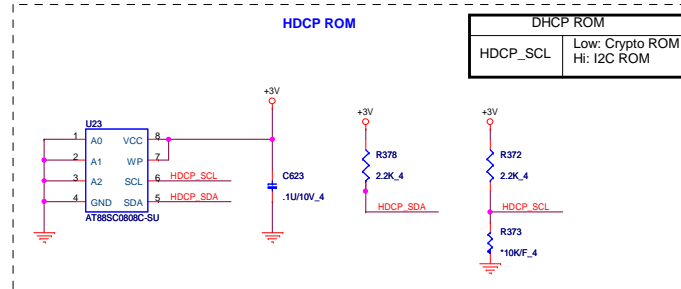
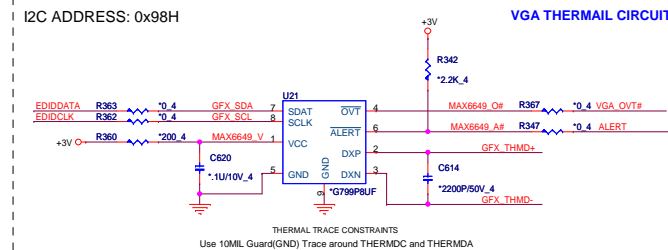
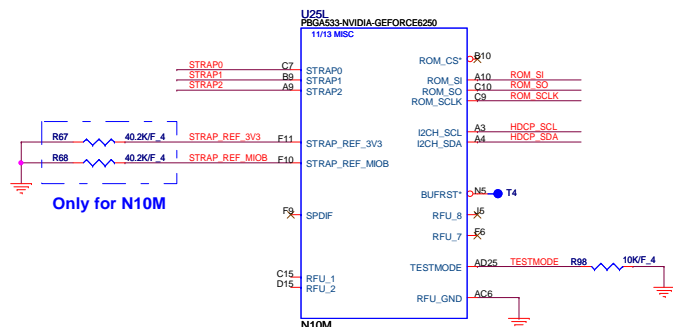




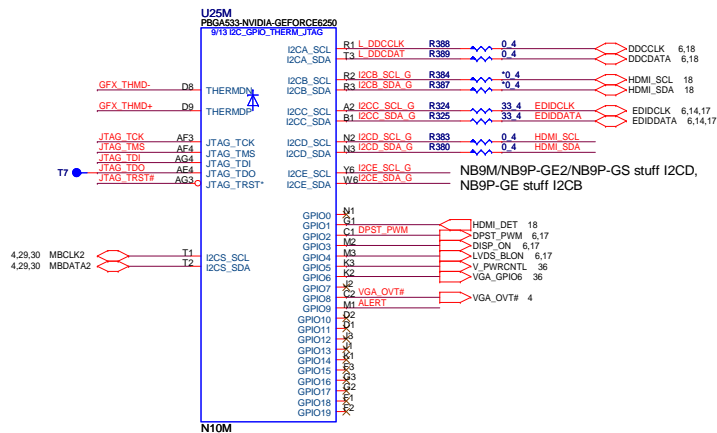
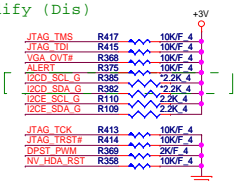
STUFF PDs on XTALSSIN and  
XTALOUTBUFF WHEN EXT\_S  
IS NOT USED

Install it when not connected to Spread spectrum device

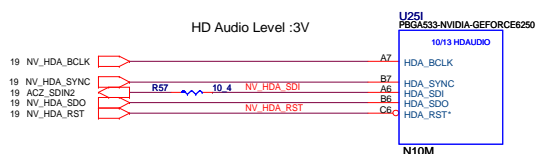




## PV Modify (Dis)



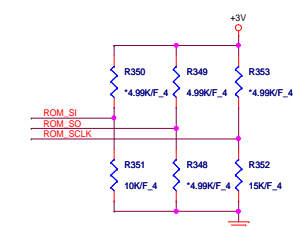
## HD Audio Level :3V



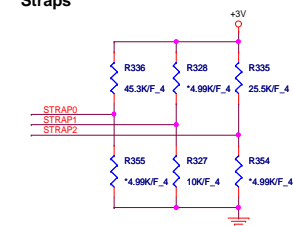
## GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL

## PCI\_DEVID[4] / SUBVENDOR



## Straps

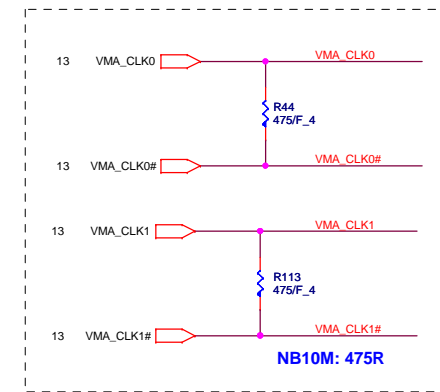
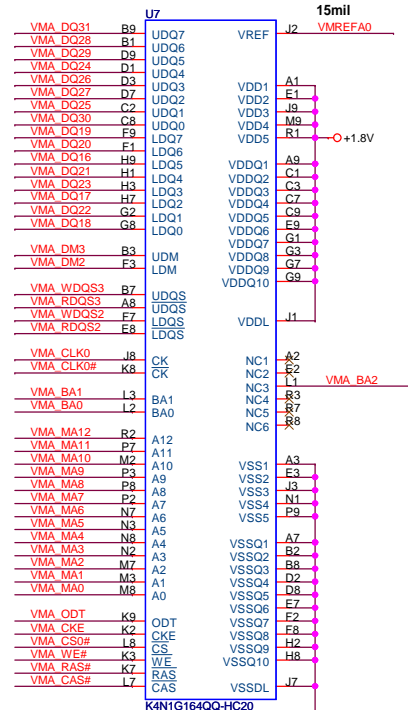
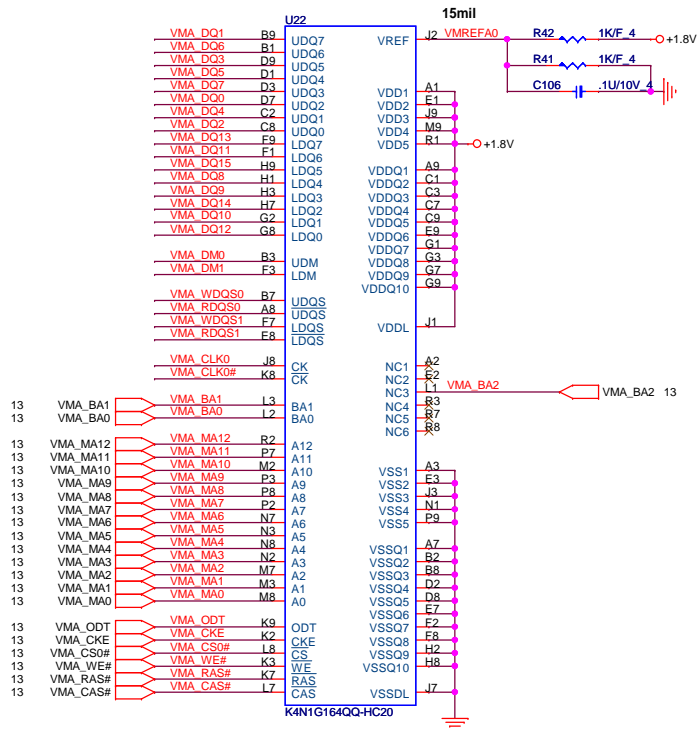


VRAM ID	
ROM_SI	PD 5K: Hynix PD 10K: Samsung PD 15K: Qimonda

## Logical Strap Bit Mapping

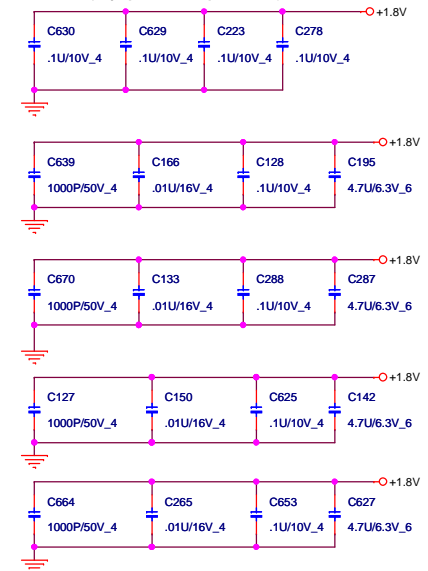
	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111





CS14752FB11 RES CHIP 475 1/16W +-1%(0402)

(By pass capacitor)



- 13 VMA\_DQ[63..0]
- 13 VMA\_DM[7..0]
- 13 VMA\_WDQS[7..0]
- 13 VMA\_RDQS[7..0]



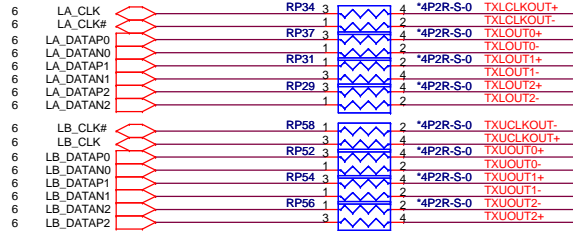
**PROJECT : Preso-II**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N10M VRAM-1(GDDR2) 5/5	1A
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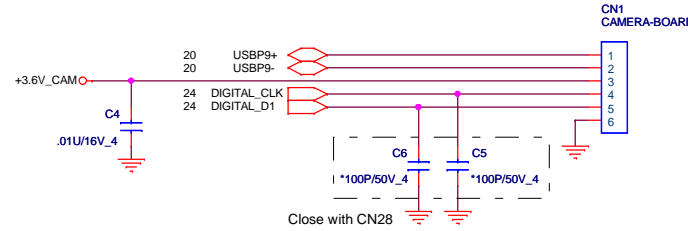
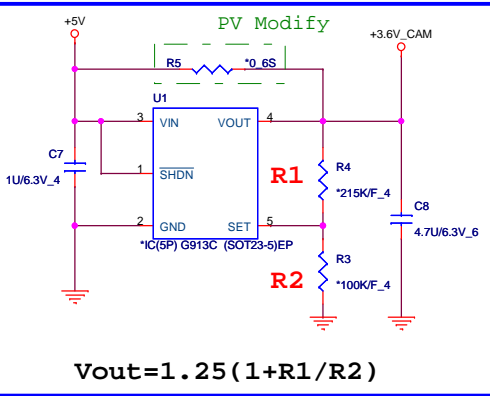
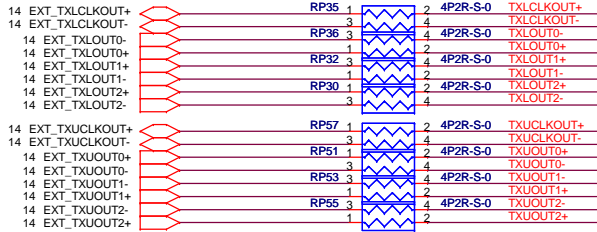


1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

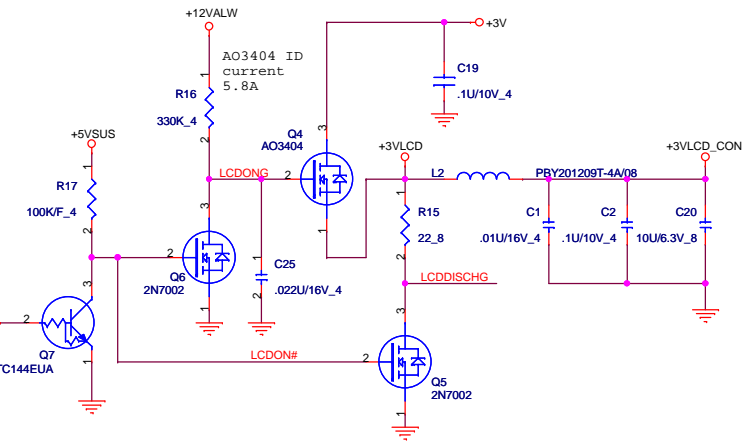
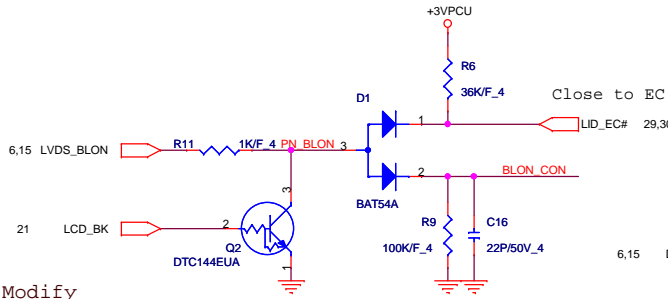
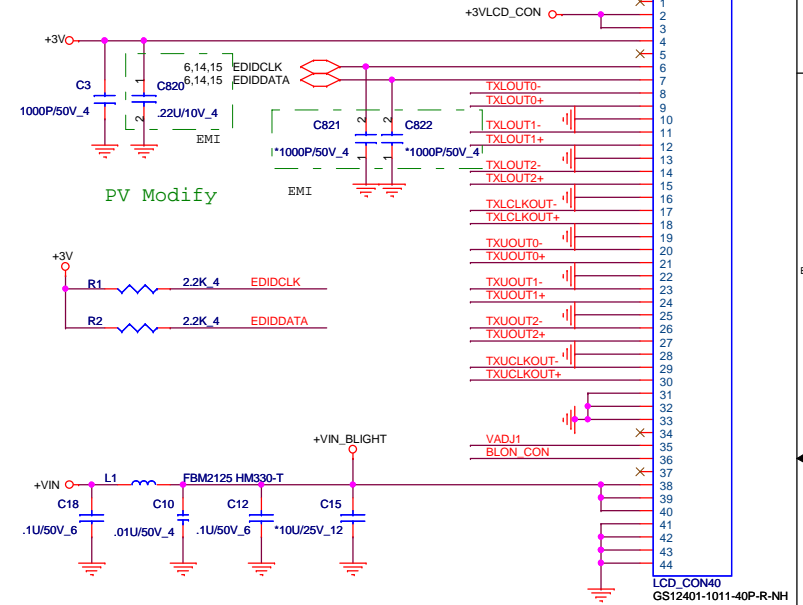
OPTION SIGNAL FROM Nb FOR UMA VGA



OPTION SIGNAL FROM Nvidia to VGA



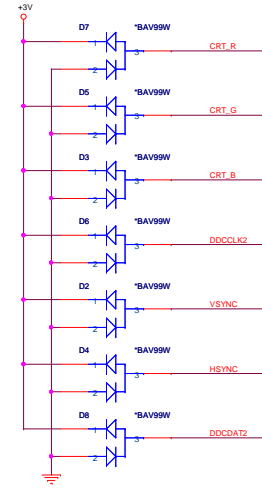
## LCD / USB CAMERA / DIGITAL MIC CONNECTOR



**PROJECT : Preso-II**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN(WC/MIC)/LID	1A
Date: Tuesday, May 05, 2009	Sheet 17 of 39	





The image displays a detailed PCB layout for an HDMI connector, organized into three main sections: a top section for signal termination and power, a middle section for signal routing, and a bottom section for power distribution.

**Top Section: Signal Termination and Power**

- Power:** A +5V\_HDMI power plane is shown at the top, connected to a D10 connector (pin 2) and an R850 (1V-40).
- Termination:** A dashed box labeled "N10M ==> 2K" and "UMA ==> 2.2K" contains two resistors: R866 (2K\_F\_4) and R390 (2K\_F\_4).
- Signal Traces:**
  - HDMI\_SCL (pin 15) and HDMI\_SDA (pin 16) are connected to R391 and R89 (33\_4) respectively, which then connect to the termination network.
  - HDMI\_SCL and HDMI\_SDA traces are shown with labels L28\_1 and L9\_1, and a value of 2 \* "0.6".
  - Capacitors C163 and C637 (10P/50V\_4) are connected to the signal lines.

**Middle Section: Signal Routing**

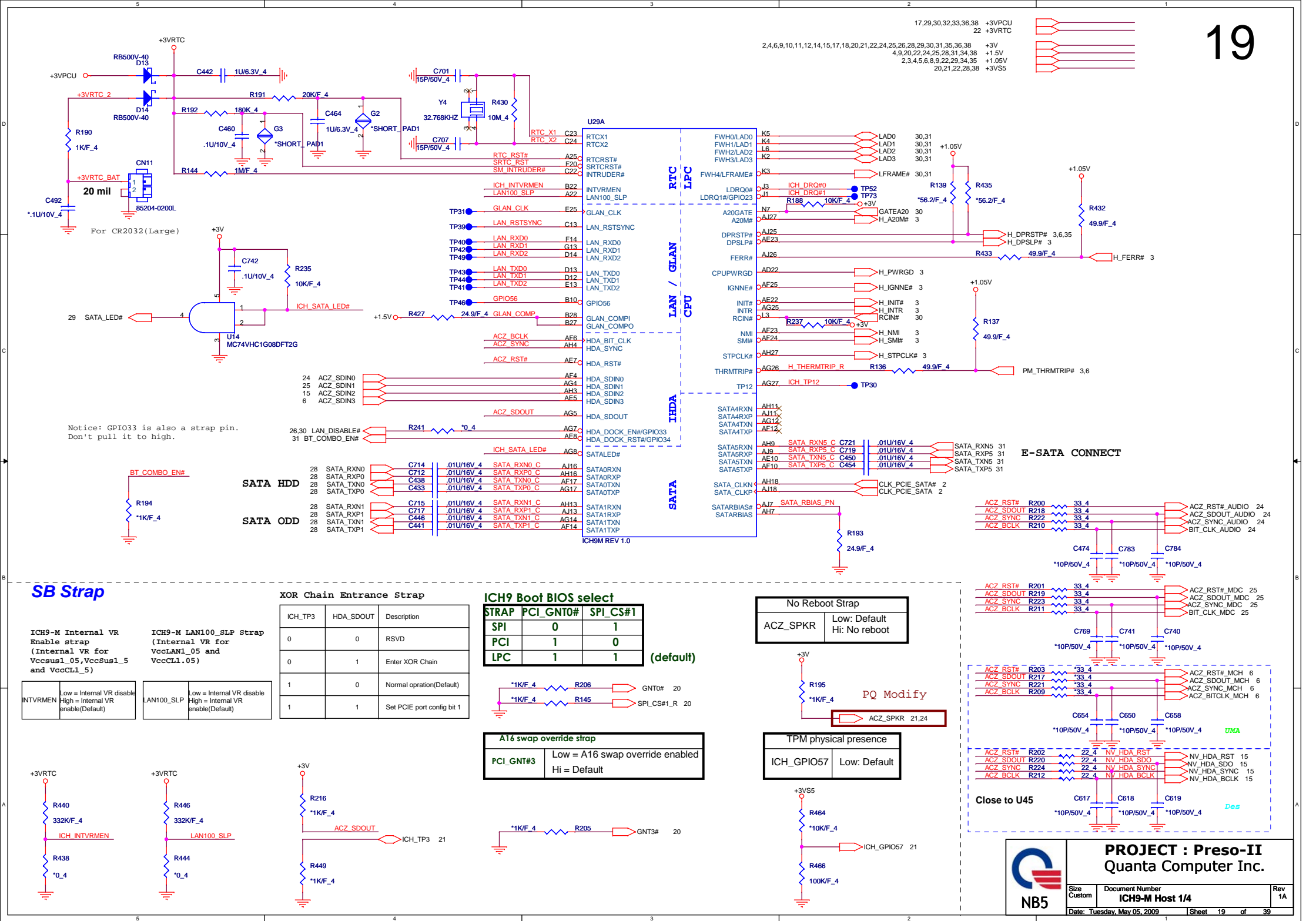
This section is labeled "Only for N10M" and shows a series of signal traces for N\_TX2\_HDMI+, N\_TX2\_HDMI-, N\_TX1\_HDMI+, N\_TX1\_HDMI-, N\_TX0\_HDMI+, N\_TX0\_HDMI-, N\_TXC\_HDMI+, and N\_TXC\_HDMI-. Each trace is connected to a specific component (C236, C243, C213, C197, C218, C238, C184, C169) and a 1U/10V\_4 capacitor. The traces are connected to the HDMI connector pins (C236, C243, C213, C197, C218, C238, C184, C169) and the HDMI connector pins (C236, C243, C213, C197, C218, C238, C184, C169).

**Bottom Section: Power Distribution**

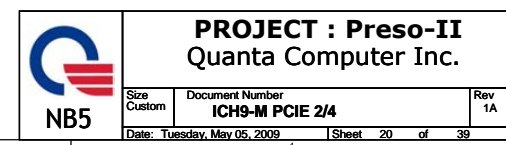
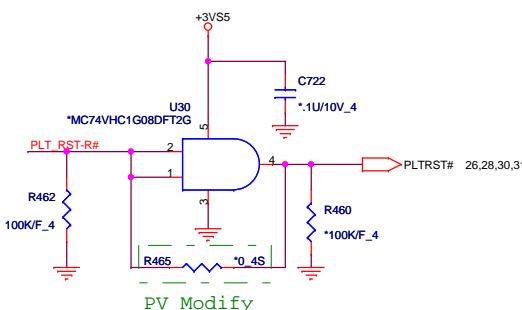
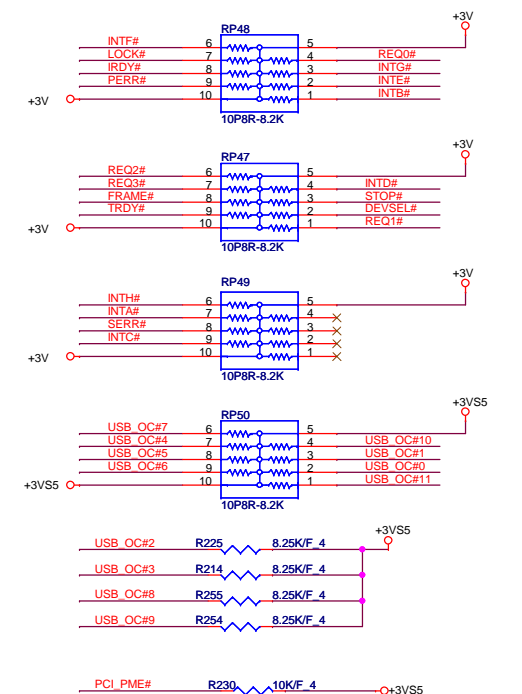
This section is labeled "Only for N10M" and shows a power distribution network. A +3V power source is connected to a D17 connector (pin 2) and a 2K7002 resistor. The power is distributed to a series of components (R406, R407, R399, R397, R402, R404, R395, R392) and a 499F\_4 capacitor. The traces are connected to the HDMI connector pins (C236, C243, C213, C197, C218, C238, C184, C169) and the HDMI connector pins (C236, C243, C213, C197, C218, C238, C184, C169).

[illegible]

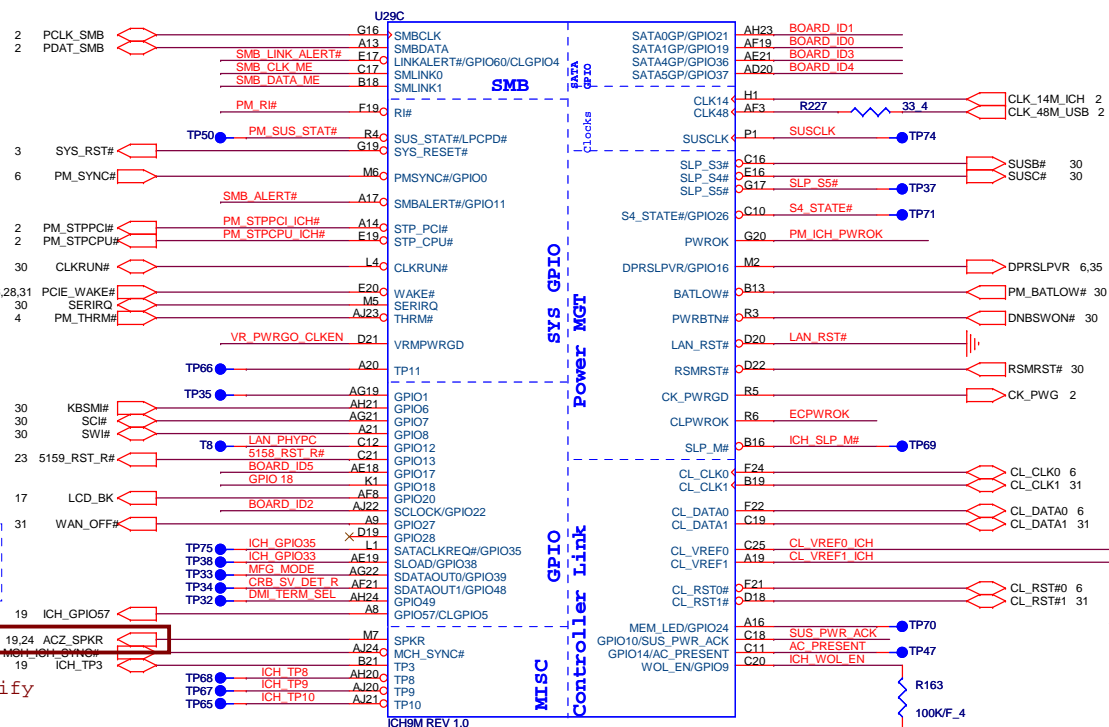




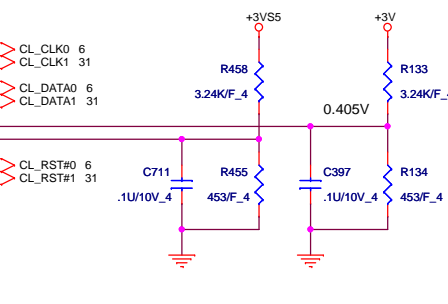






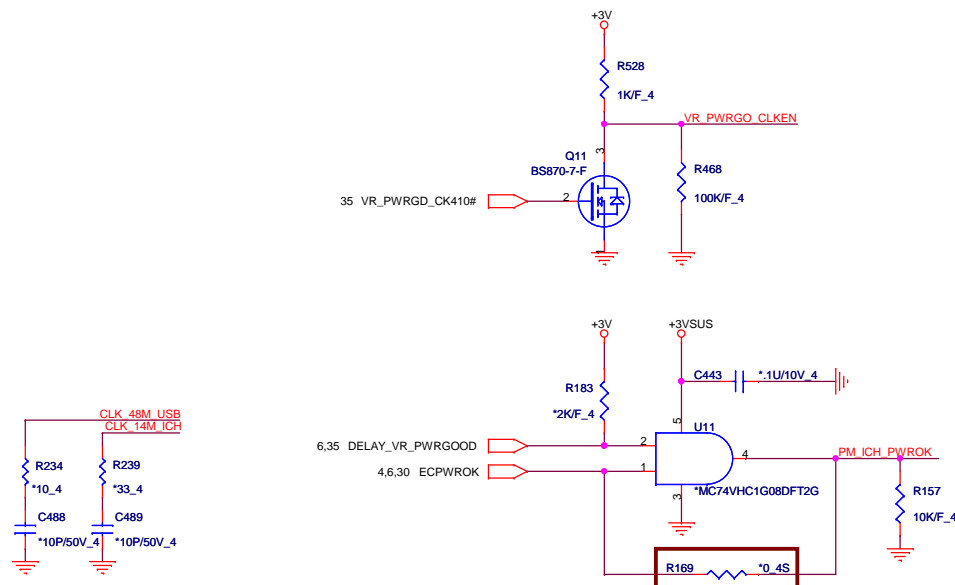


PQ Modify



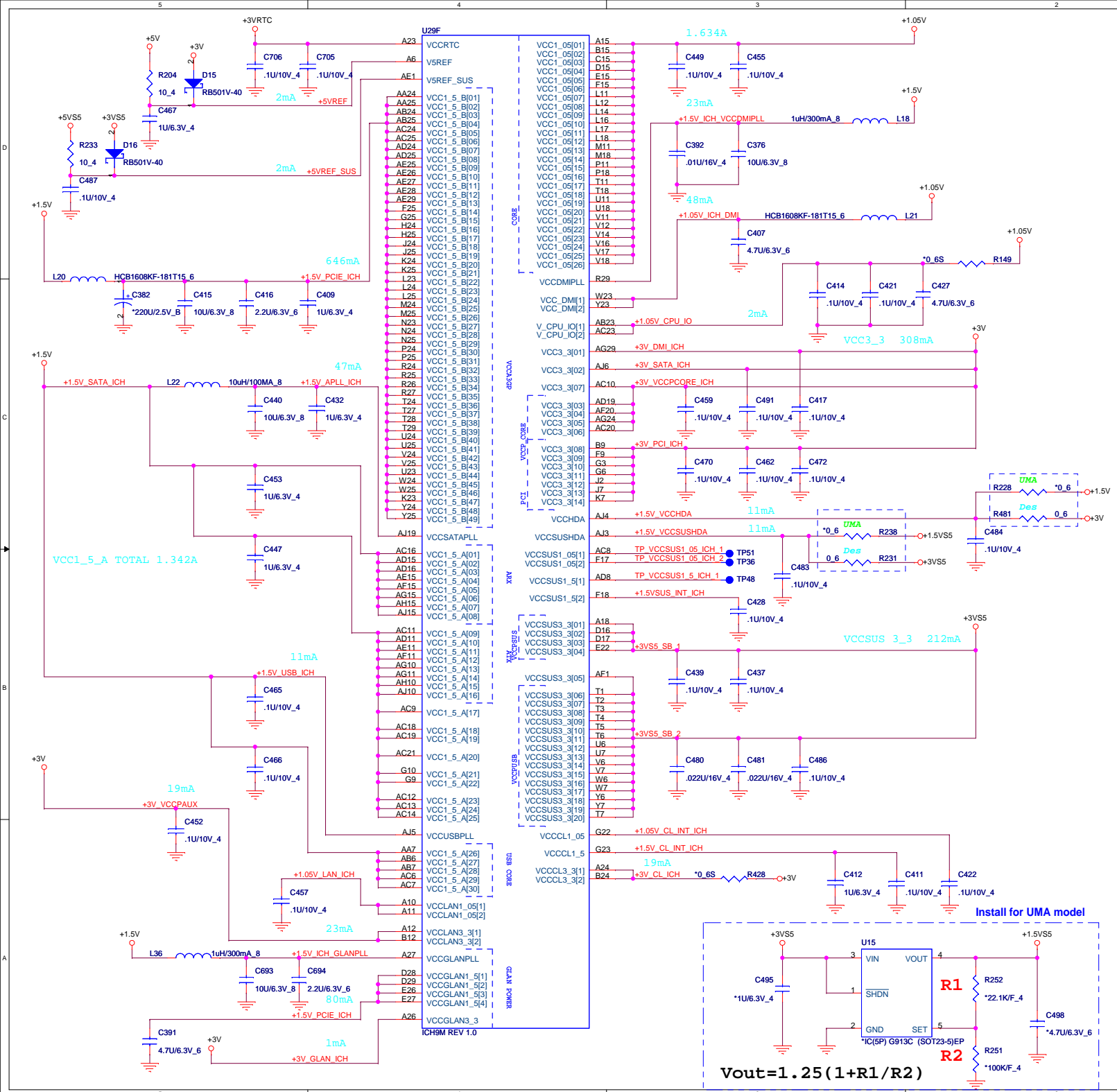
PV Modify

Model	BOARD_ID 2	BOARD_ID 3	BOARD_ID 5
GM45	0	0	1
GL40	0	0	1
N10M	1	0	1

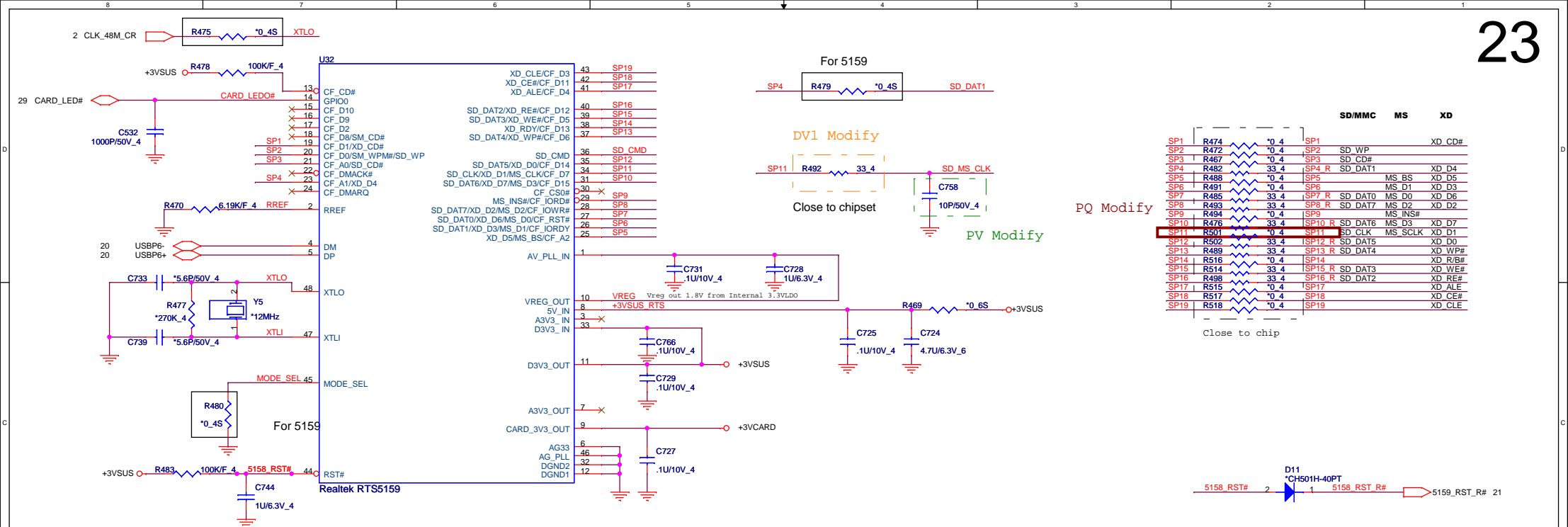


PQ Modify

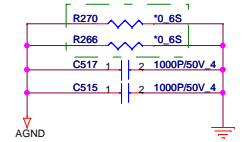




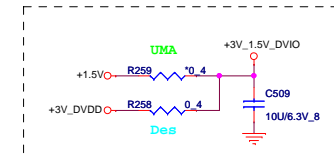
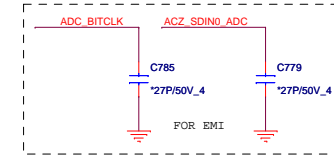




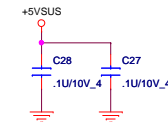
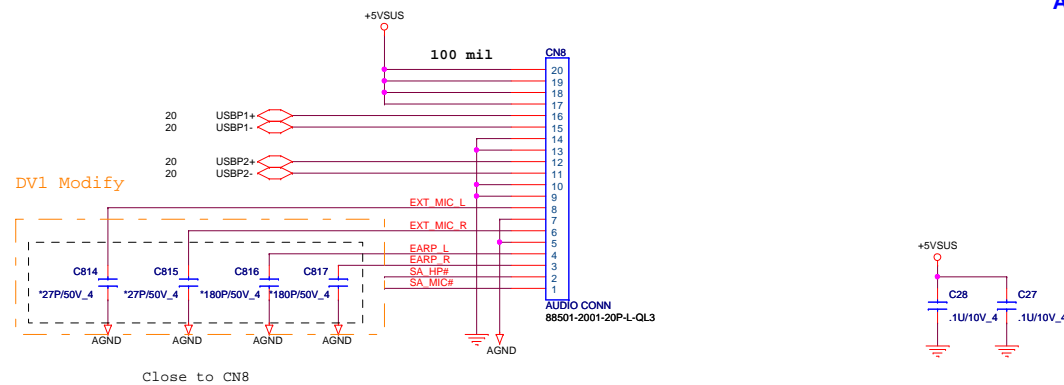




PORT	PLACE TO
MONO_OUT	X
PORT A	X
PORT B	Audio Jack MIC
PORT C	X
PORT D	Internal Speakers
PORT E	X
PORT F	X
PORT I	HP OUT

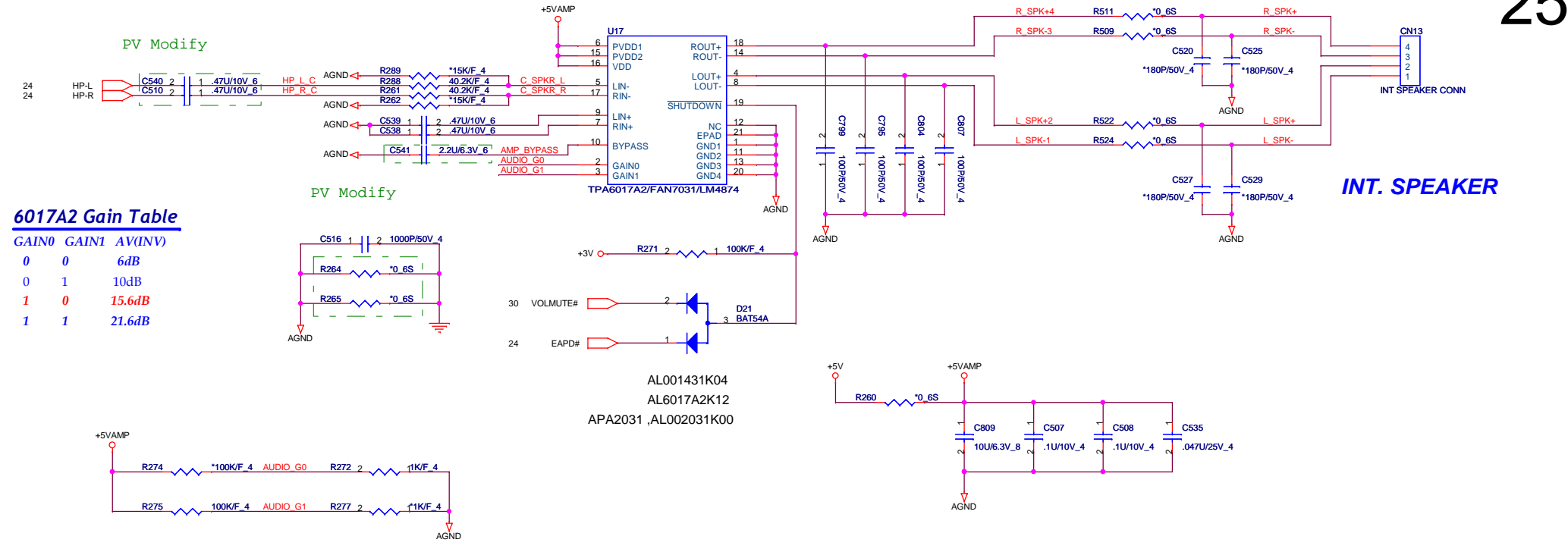


## AUDIO / USB BOARD CONNECTOR



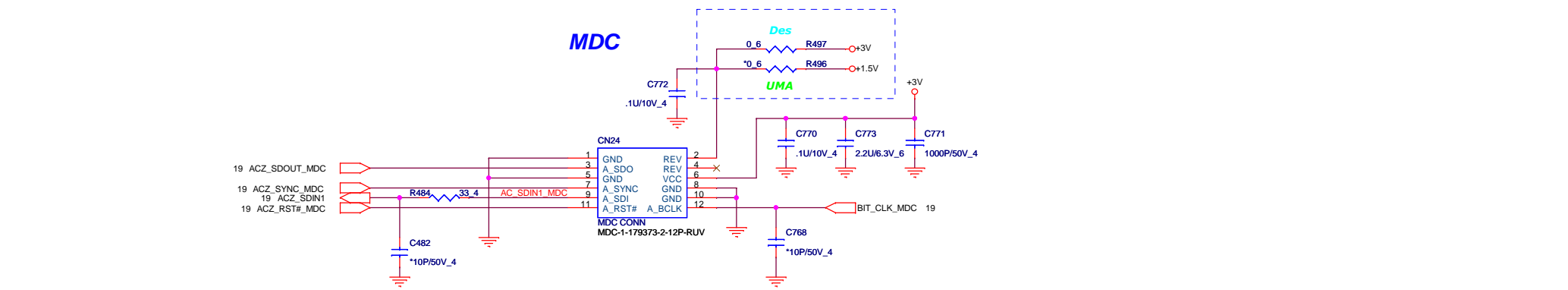


AUDIO AMPLIFIER

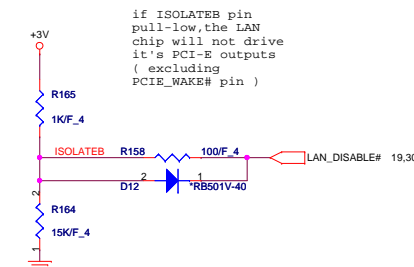
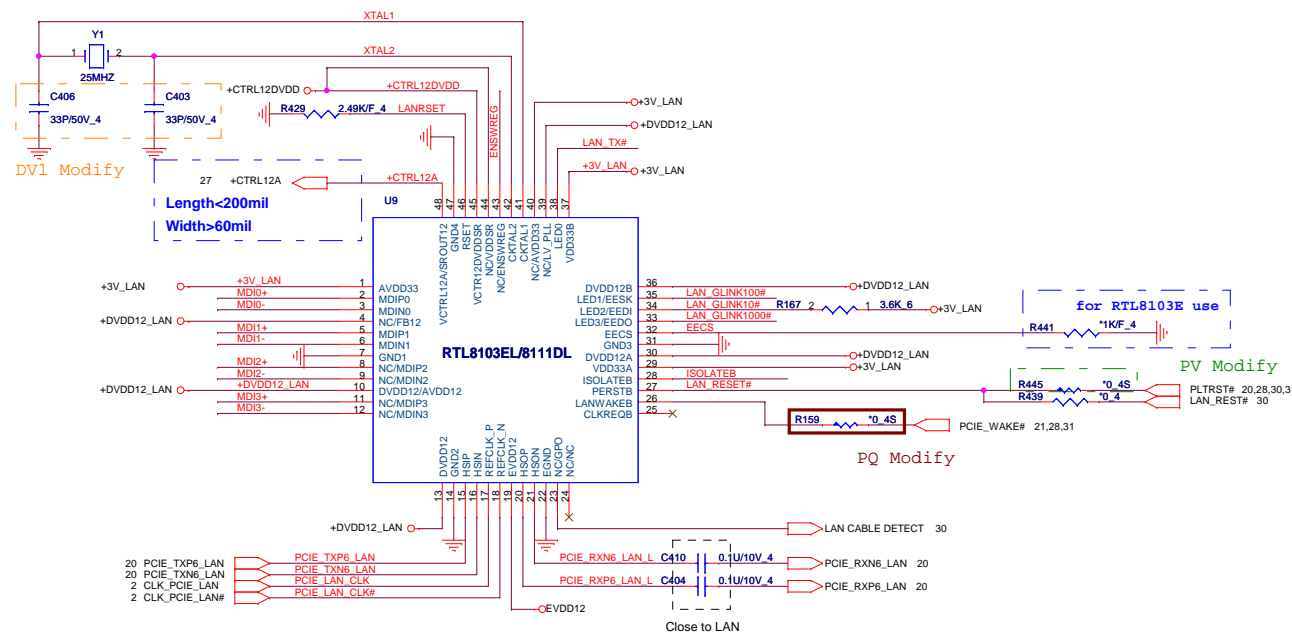
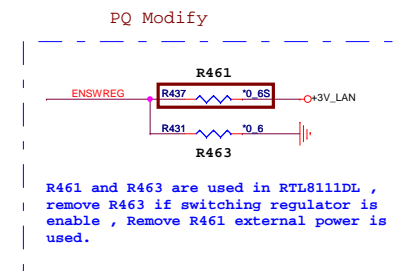
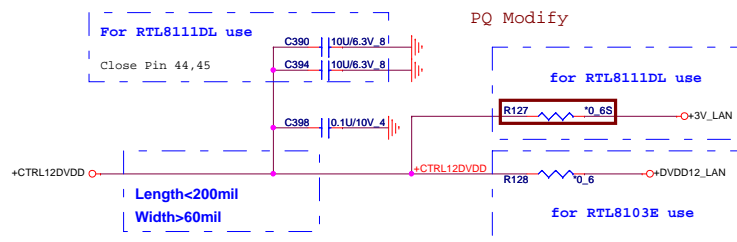


**6017A2 Gain Table**

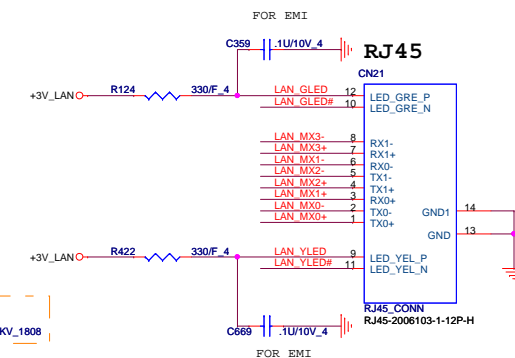
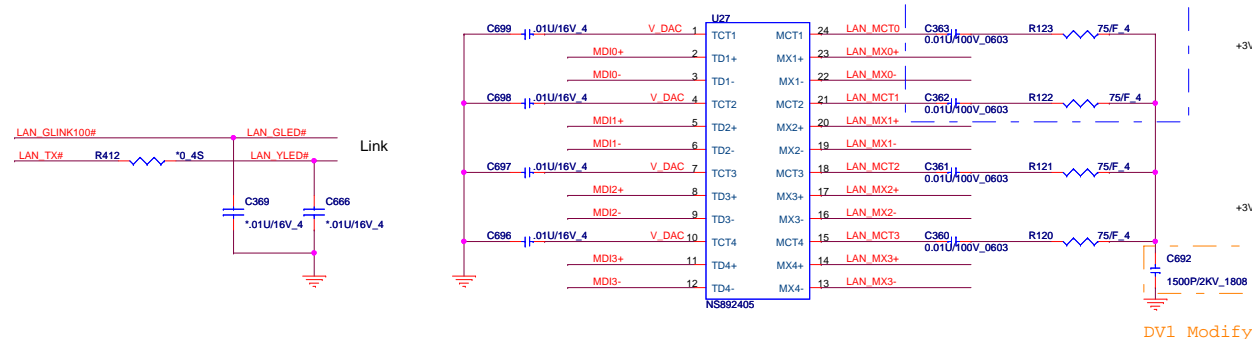
GAIN0	GAIN1	AV(INV)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB





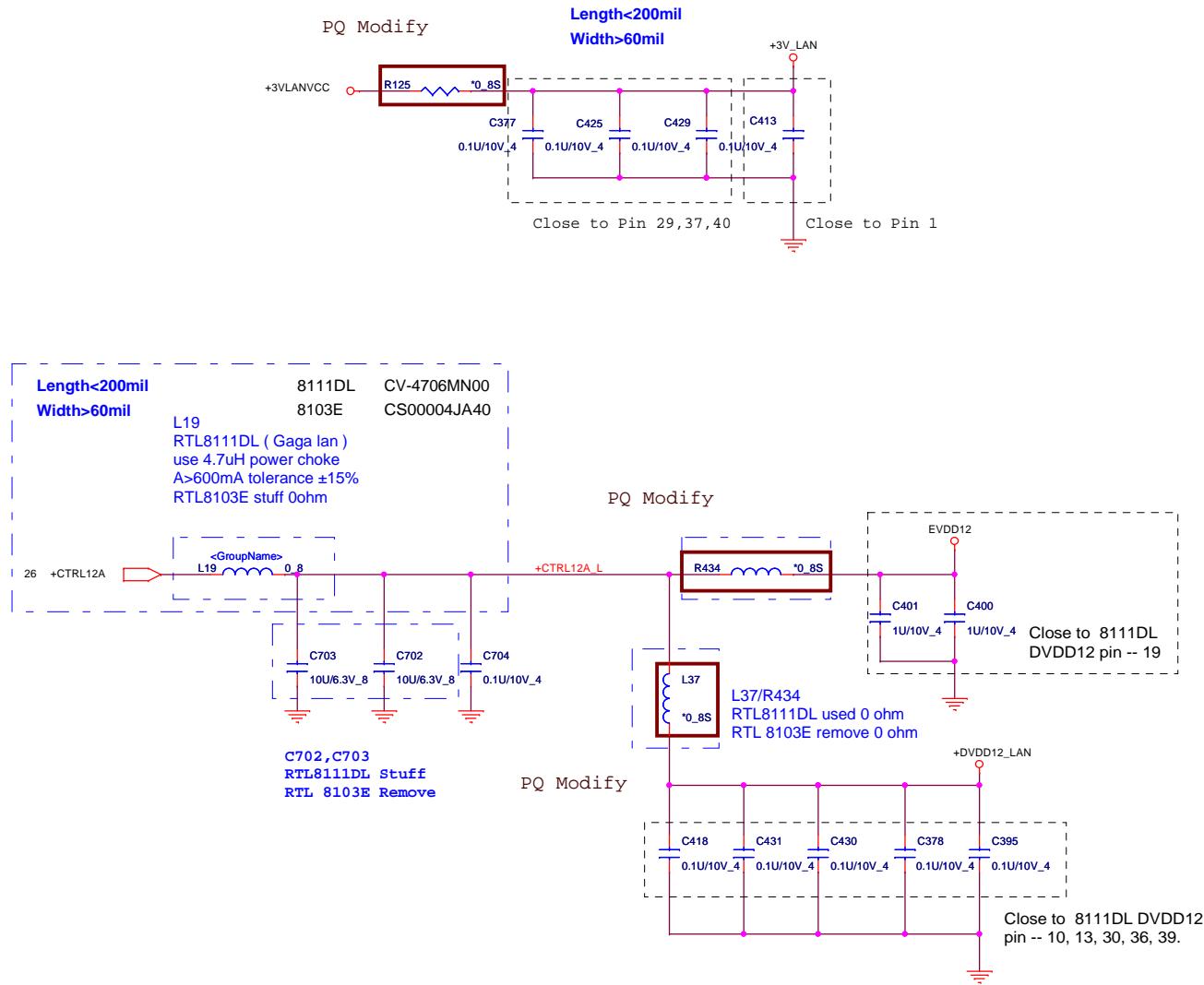


AL08111DB00	RTL8111DL-GR
AL08103EB00	RTL8103EL-GR



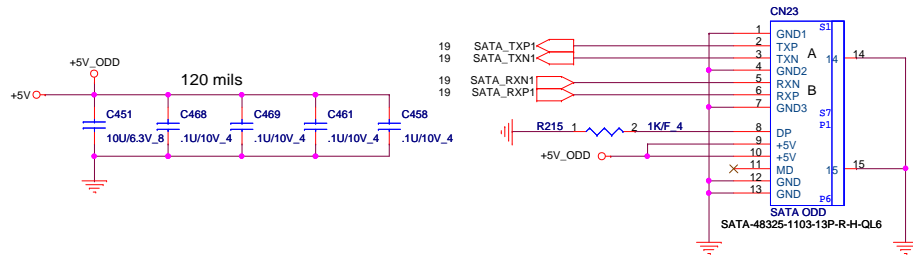
NS892402:1G	DB0AT9LAN05
NS892405:10/100	DB0ZB1LAN04



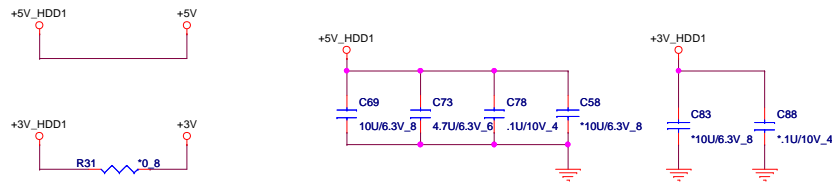
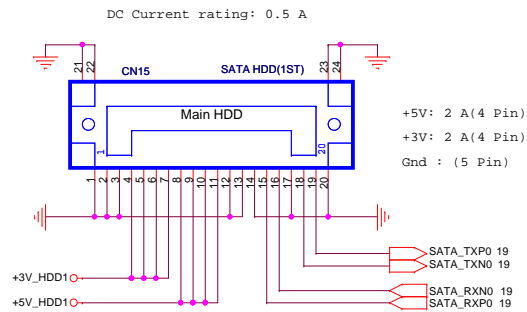




## SATA ODD CONECTOR

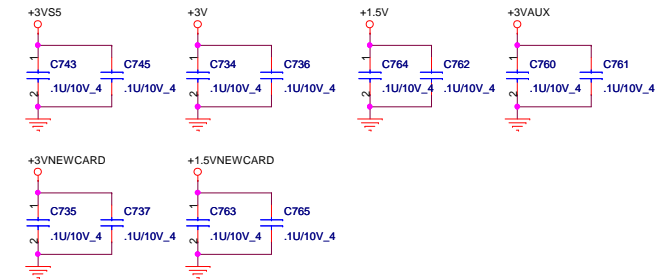
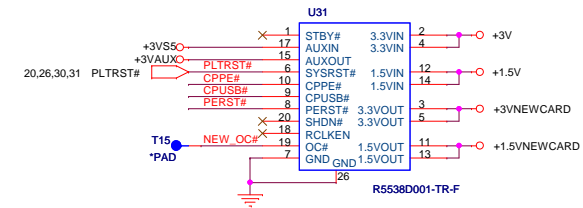
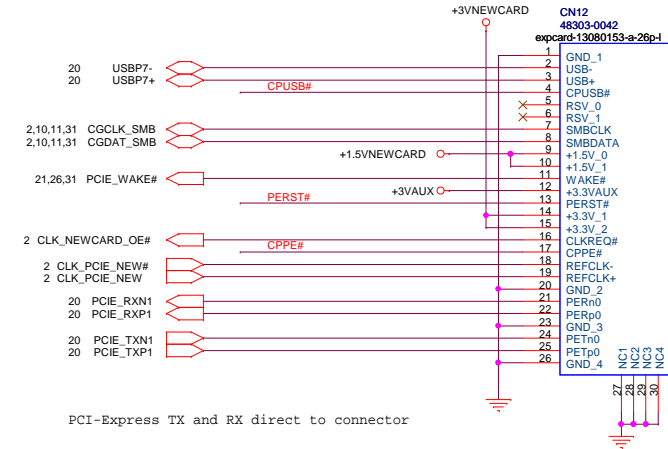


## SATA HDD CONNECTOR



NEWCARD

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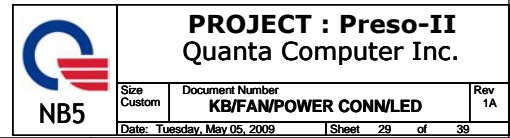
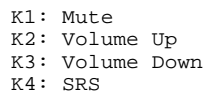




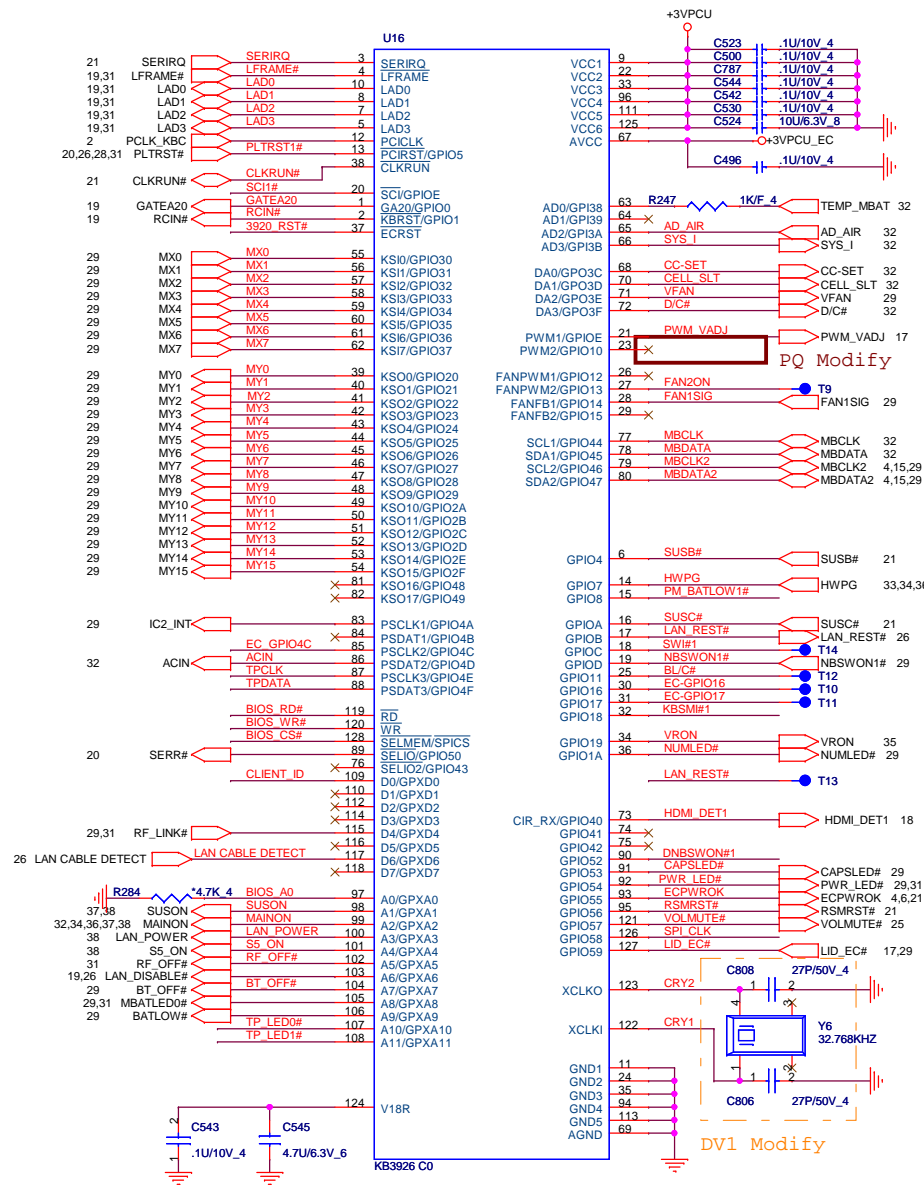
[illegible]

The diagram shows the internal wiring of the 88767-25 connector. It features two 8-pin headers (RP40 and RP41) and two 8-pin connectors (10P8R-8.2K). The connections are as follows:

- RP40 Header:**
  - Pin 1: MY3
  - Pin 2: MY2
  - Pin 3: MY1
  - Pin 4: MY0
  - Pin 5: (unconnected)
  - Pin 6: MY7
  - Pin 7: MY6
  - Pin 8: MY5
  - Pin 9: MY4
  - Pin 10: (unconnected)
- RP41 Header:**
  - Pin 1: MY11
  - Pin 2: MY10
  - Pin 3: MY9
  - Pin 4: MY8
  - Pin 5: (unconnected)
  - Pin 6: MY15
  - Pin 7: MY14
  - Pin 8: MY13
  - Pin 9: MY12
  - Pin 10: (unconnected)
- 10P8R-8.2K Connectors:**
  - Connector 1 (top): Pin 10 is connected to +3VPCU. Pin 1 is connected to MY3.
  - Connector 2 (bottom): Pin 10 is connected to MY12. Pin 1 is connected to MY11.
- External Connections:**
  - Pin 30: MY[0..15] (blue line)
  - Pin 30: MX[0..7] (blue line)

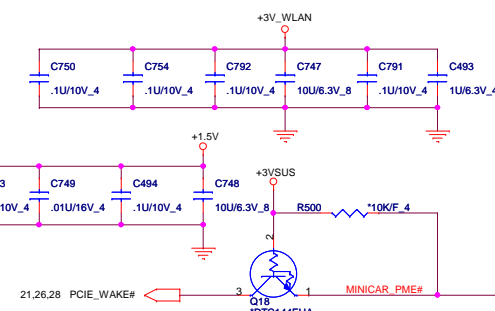
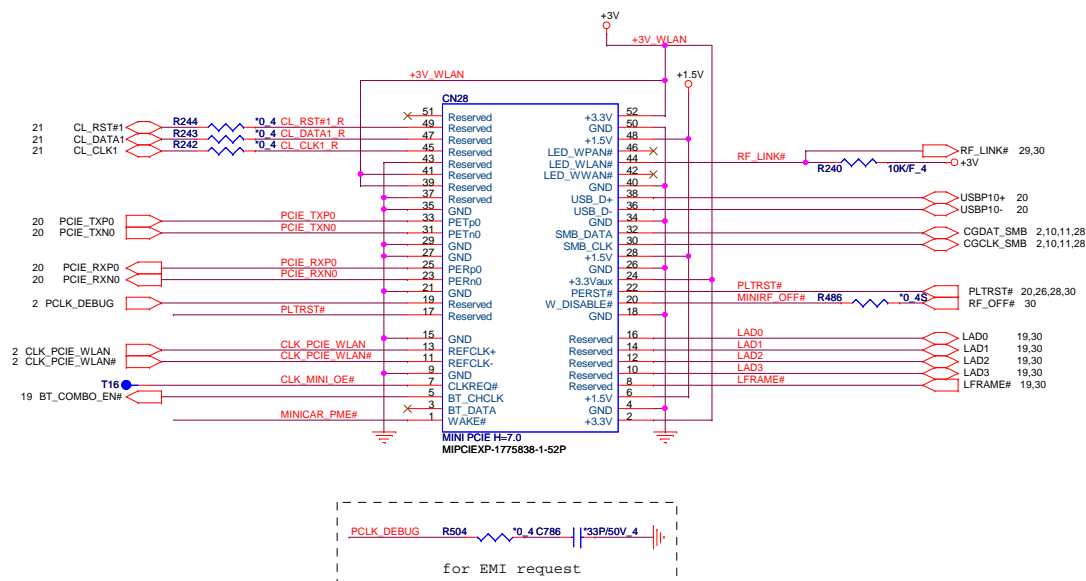




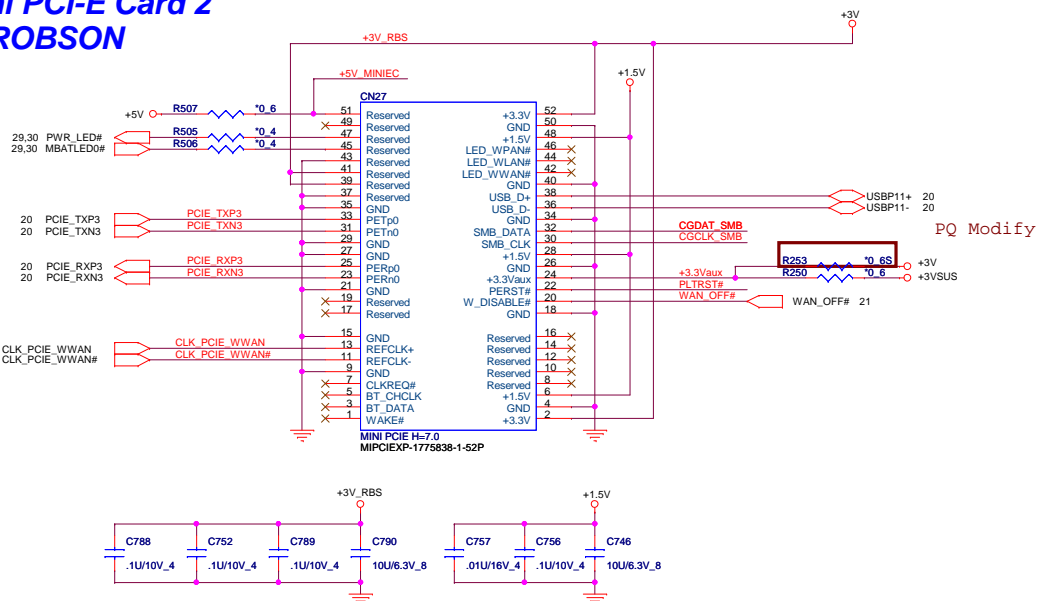




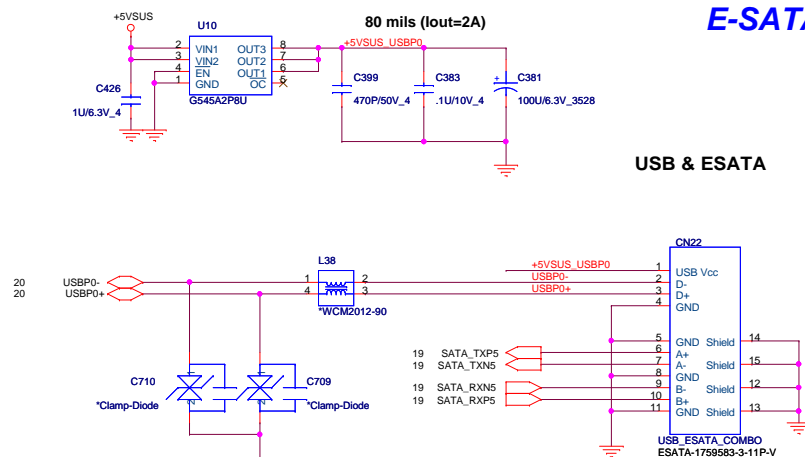
### Mini PCI-E Card 1 WLAN



## Mini PCI-E Card 2



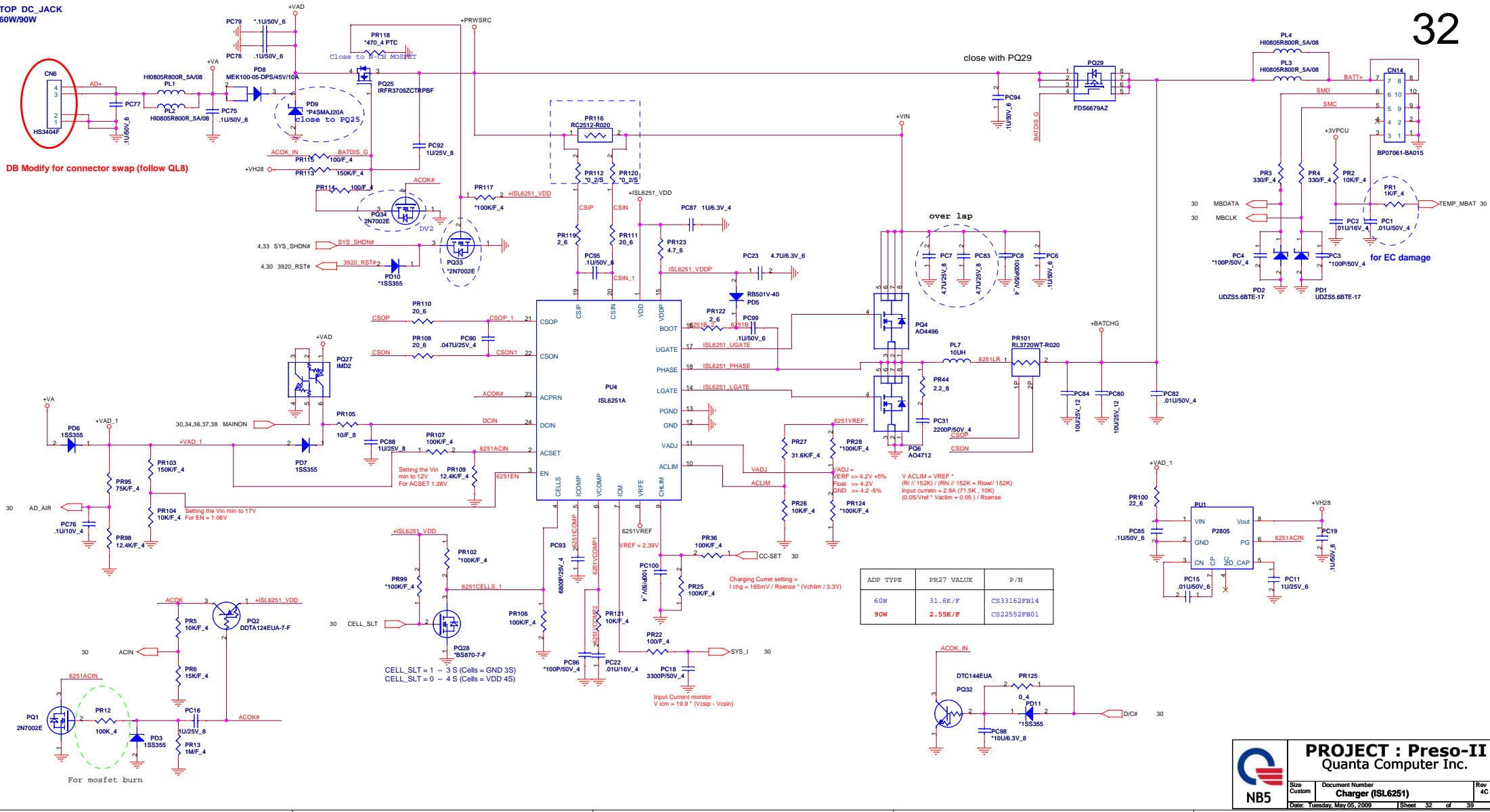
### E-SATA/USB COMBO






TOP DC JACK  
60W/90W

DB Modify for connector swap (follow QL8)



ADP TYPE	PR27 VALUE	P/N
60W	31.6K/F	CS33162FB14
90W	2.55K/F	CS22552FB01

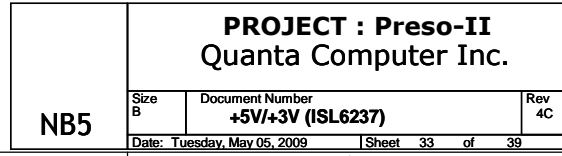


**PROJECT : Preso-II**  
Quanta Computer Inc.

Size Custom    Document Number **Charger (ISL6251)**    Rev 4C

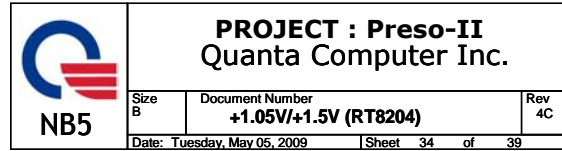
Date: Tuesday, May 05, 2009    Sheet 32 of 39







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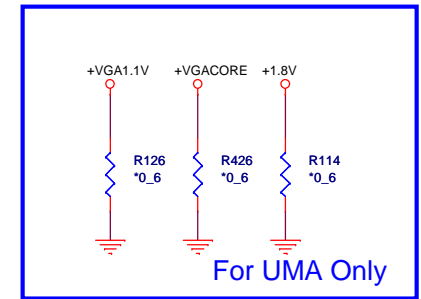
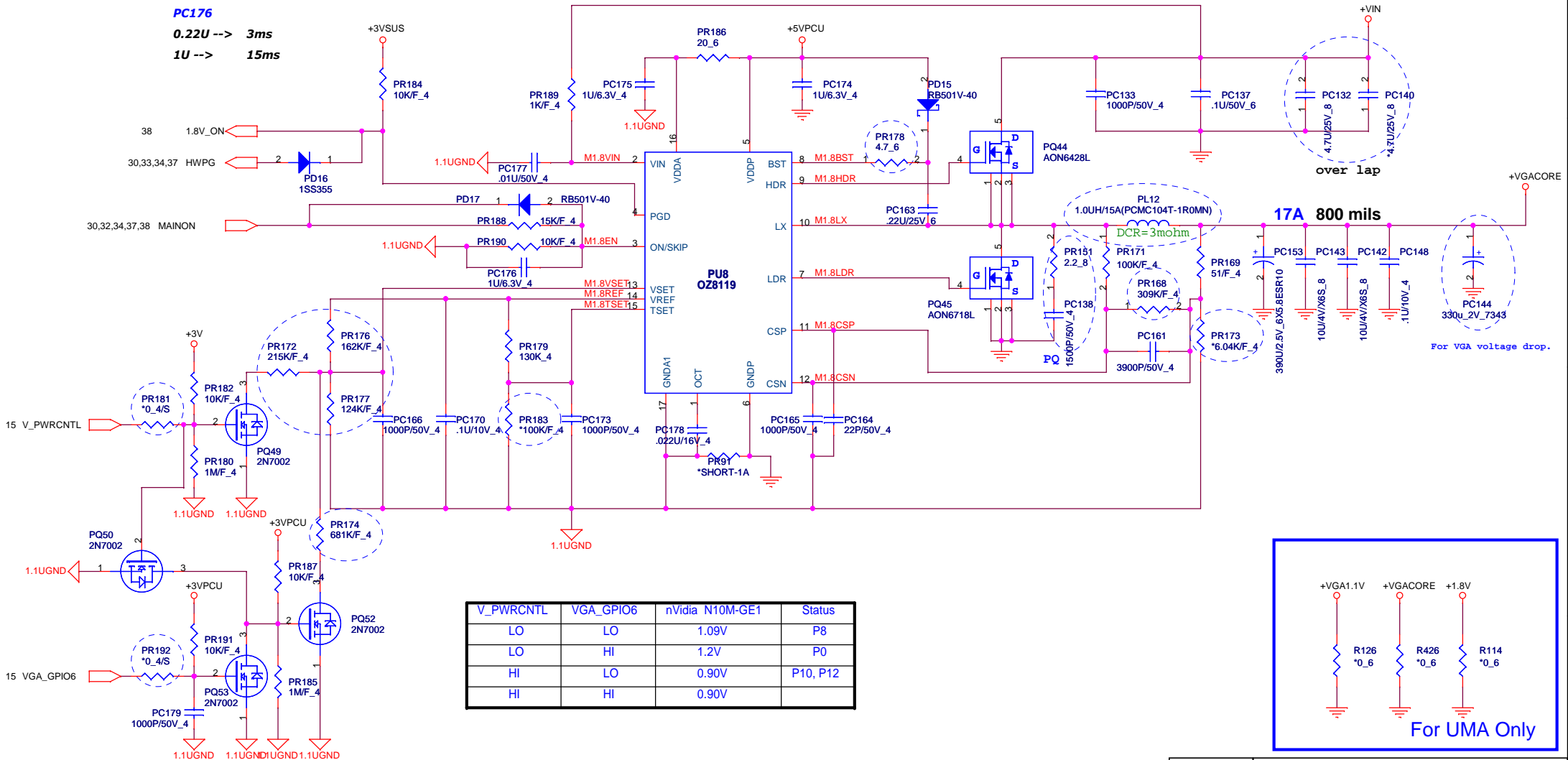
# VGA Core & VCC1.1

+1.1Volt +/- 5%  
 Countinue current:15A  
 Peak current:17A  
 OCP minimum 22A

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PC176

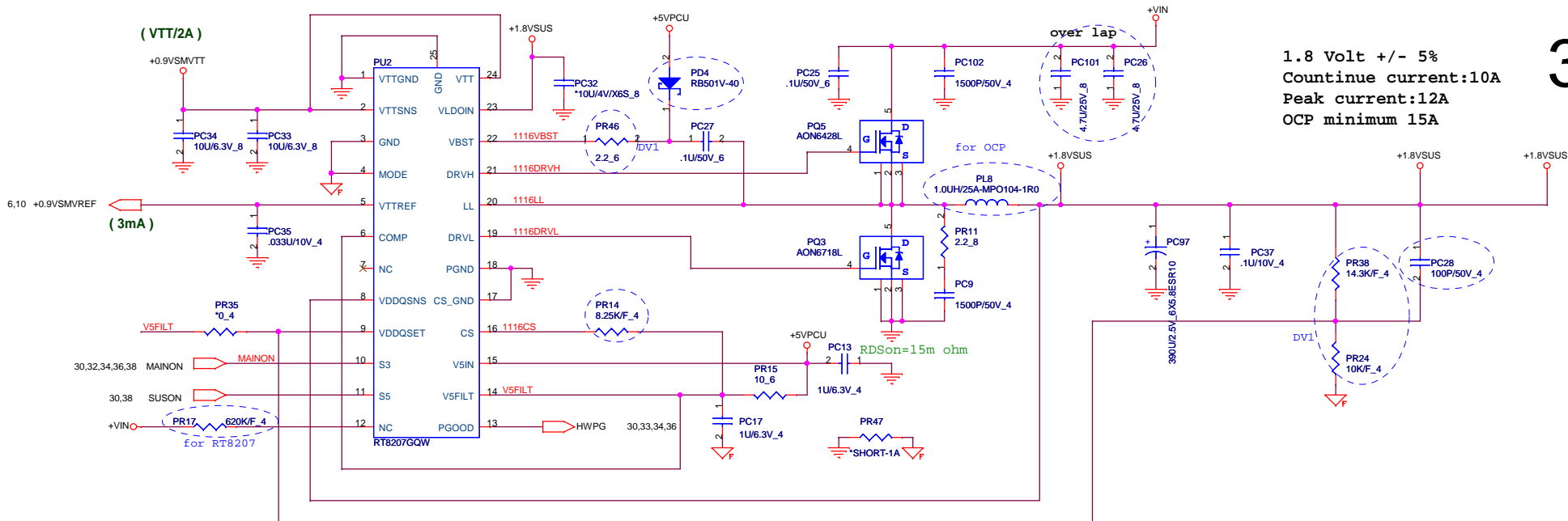
0.22U --> 3ms  
 1U --> 15ms



**PROJECT : Preso-II**  
 Quanta Computer Inc.

Size	Document Number	Rev
B	VGA CORE OZ8119	4C
Date: Tuesday, May 05, 2009 Sheet 36 of 39		

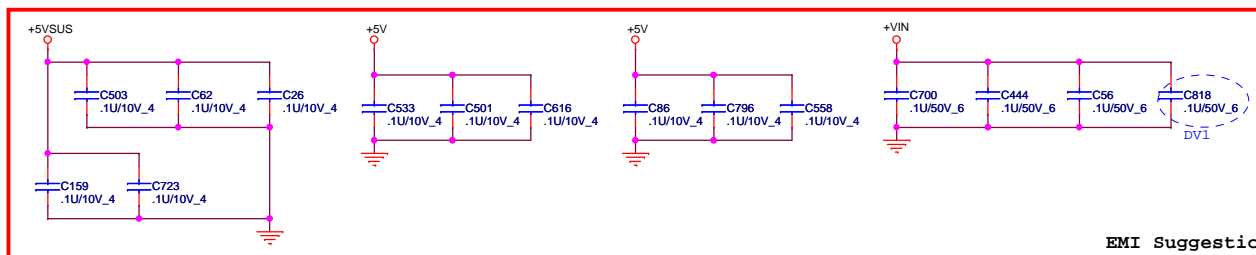
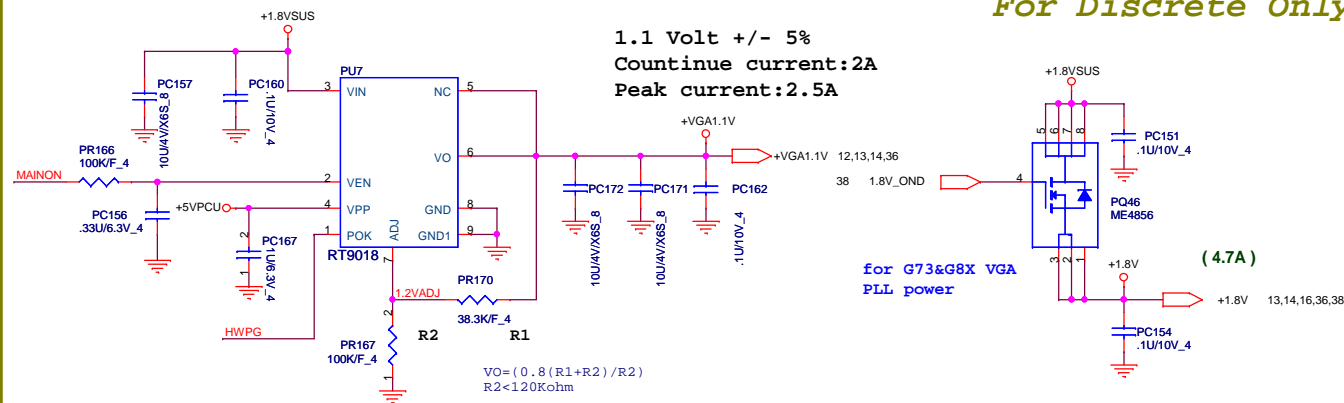




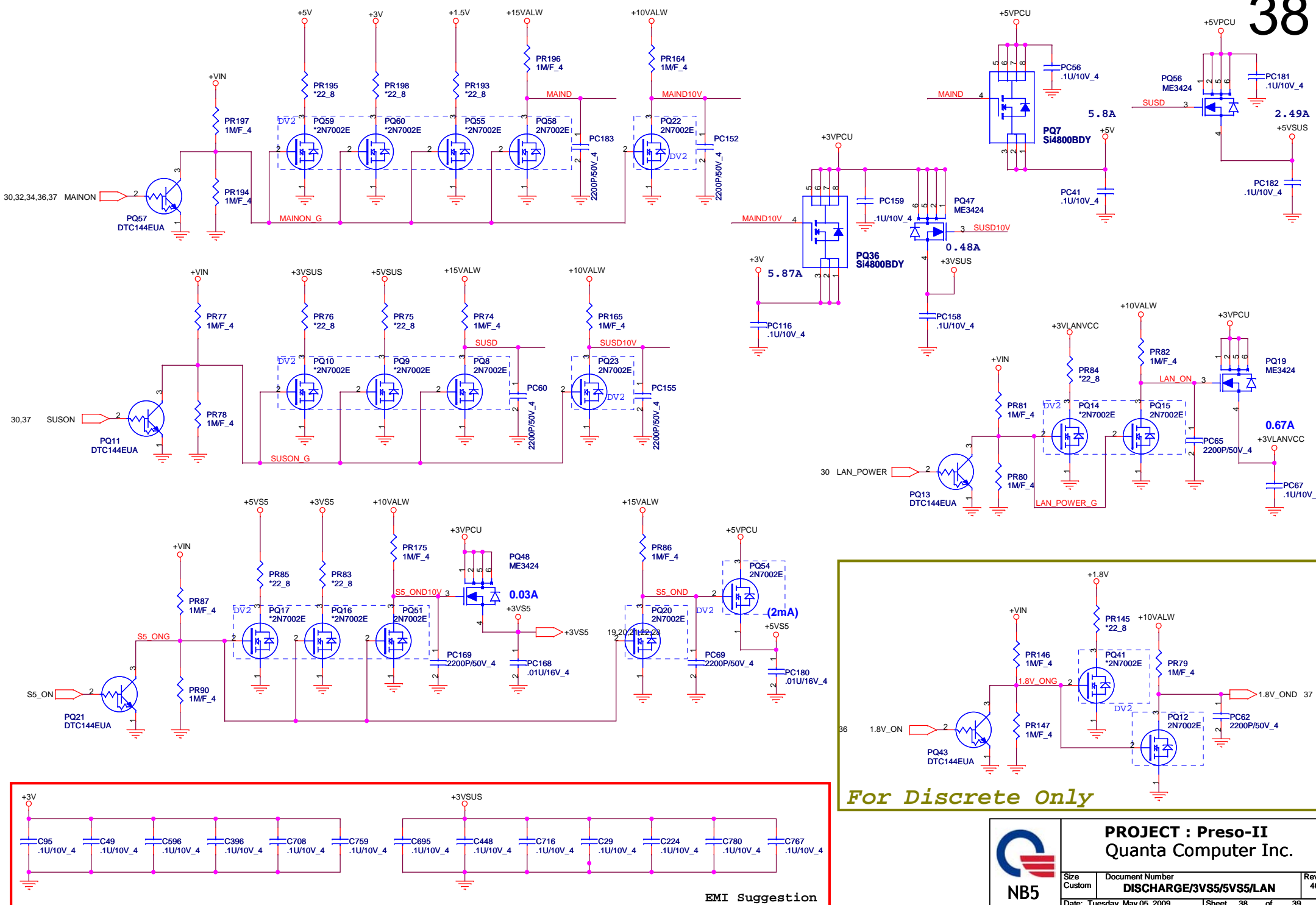
1.8 Volt +/- 5%  
 Countinue current:10A  
 Peak current:12A  
 OCP minimum 15A

### For Discrete Only

1.1 Volt +/- 5%  
 Countinue current:2A  
 Peak current:2.5A









		AC MODE				DC MODE			
	Voltage level	S0	S3	S4	S5	S0	S3	S4	S5
+3VPCU	3.3V +/- 5%	V	V	V	V	V	V	V	V
+5VPCU	5V +/- 5%	V	V	V	V	V	V	V	V
+3VRTC	3.3V +/- 5%	V	V	V	V	V	V	V	V
+3VS5	3.3V +/- 5%	V	V	V	V	V	V		
+5VS5	5V +/- 5%	V	V	V	V	V	V		
+3VSUS	3.3V +/- 5%	V	V			V	V		
+5VSUS	5V +/- 5%	V	V			V	V		
+1.8VSUS	1.8V +/- 5%	V	V			V	V		
+0.9VSMVTT	0.9V +/- 5%	V	V			V	V		
+1.5V	1.5V +/- 5%	V				V			
+1.05V	1.05V +/- 5%	V				V			
+VCORE	0.9~1.15V	V				V			
+VGA_CORE	0.9~1.2V	V				V			
+VGA1.1V	1.1V +/- 5%	V				V			
+1.8V	1.8V +/- 5%	V				V			
+3VLAVCC	3.3V +/- 5%	V				V			



**PROJECT : Preso-II**  
Quanta Computer Inc.

Size  
Custom

Document Number  
**Voltage status**

Rev  
1A

Date: Monday, May 04, 2009

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